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Cryogenic Millimeter-Wave CMOS Low-Noise Amplifier

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***Abstract*— In this paper we report a cryogenically cooled CMOS amplifier covering at least 75 to 115 GHz frequency range. The amplifier chip was fabricated in 28-nm FD SOI CMOS technology. When cryogenically cooled to 20 K and measured on-wafer the CMOS amplifier shows 108-155 K noise temperature from 75 to 115 GHz. This means 6 to 8 times improvement in noise temperature compared to room temperature noise. The measured small-signal gain is around 20 dB. To the best of authors' knowledge, these are the first cryogenic measurements of millimeter-wave CMOS amplifiers and lowest CMOS LNA noise temperatures for W-Band reported to date.**

***Index Terms*— CMOS, Cryogenic, low-noise amplifiers, MMIC**

I. Introduction

Cryogenically cooling of low-noise amplifiers leads to large reduction in noise and is used to improve the sensitivity of receiver systems in applications such as radio astronomy and Earth observation systems. At millimeter-wave frequencies the lowest noise performance have been obtained with HEMT amplifiers [1]-[4]. At lower frequencies (< 10 GHz) silicon germanium (SiGe) heterojunction bipolar transistors have emerged as an attractive option for used in cryogenic low-noise systems [5]-[7]. Furthermore, a SiGe Ka-band cryogenic amplifier was reported in [8]. In [9] cryogenic performance of 32-nm SOI CMOS devices was reported and it was found out that the noise performance of SOI CMOS devices is very competitive with other technologies in microwave frequency range. Since CMOS amplifiers have shown good performance at millimeter-wave frequencies [10][11] and even around 200 GHz [12] it is tempting to study the operation of CMOS millimeter-wave amplifier at cryogenic temperatures. In this work, we report cryogenically cooled W-band CMOS amplifier.

II. CMOS Amplifier Design

The detailed design of the amplifier was presented in [11]. The amplfier was manufactured in a 28-nm FDSOI CMOS technology. The back-end metallization consists of ten copper layers and a thick aluminum top metal. A three-stage amplifier was designed in a common source configuration and in a microstrip environment. The simplified schematic of the LNA is shown in Fig. 1 and a micrograph in Fig. 2. A simple T-type matching network was used for input matching to minimize the loss of the matching circuitry. At the same time the size of the input stage transistor was optimized to obtain a wideband noise match. Furthermore, source degeneration was used for the input transistor to achieve optimum noise match with good input match. The interstage matching network consists of series transmission lines and short-circuited shunt stubs. For wideband output matching an additional open stub was used. DC-blocking capacitors are used only at the input and output of the amplifier to avoid potential modeling errors and loss of these series capacitors. Low frequency stability was ensured by RC networks at the bias lines. It should be noted that the amplifier was optimized for room temperature operation and no attempt was made to model the performance at cryogenic temperatures.

The measured room temperature small-signal gain of the amplifier was 12 dB with better than 10-dB input and output return losses from 53 to 117 GHz. The measured noise figure was 6 dB from 75 to 105 GHz.

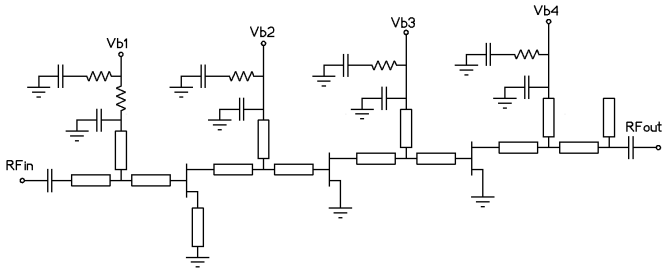

Fig. 1. Simplified schematic of the CMOS low-noise amplifier (reproduced from [11]).

III. Cryogenic Measurements

The amplifier was measured cryogenically on-wafer in a Cryogenic Probe Test Station (CPTS) presented in [13][14]. Fig. 2 shows an image of the amplifier being probed in the CPTS.

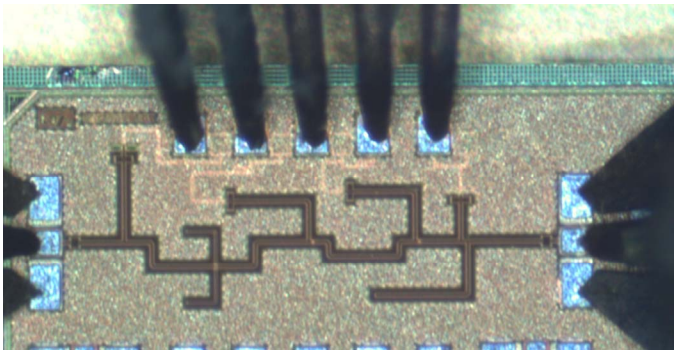

Fig. 2. CMOS LNA undergoing cryogenic wafer probing. The chip size of the CMOS LNA is 1140 µm x 400 µm.

Two amplifier chips were first affixed to a separate carrier with conductive epoxy and this carrier was clamped to the 19 K CPTS chuck, with a layer of indium between them to ensure good thermal contact. A heater attached to a waveguide termination connected to the input waveguide probe provided the variable-temperature load needed for a Y-factor measurement. Since we do not correct for the loss in the input waveguide probe, the noise temperatures from this measurement will systematically over-estimate the true noise temperature. By comparing measurement in the CPTS to those of the same chips packaged in WR-10 housings, we have determined that the CPTS noise temperatures are overestimated by about 10-20% (in plots of the CPTS noise temperatures shown here, we do not attempt to correct for this effect).

The output wafer probe is connected to a cooled isolator and RF backend amplifier, which connects via waveguide to the Dewar wall. Outside the Dewar, an isolator is followed by a double sideband heterodyne receiver, IF amplifiers and filters. A commercial power sensor measures the IF power at each frequency. By connecting the input and output wafer probes via a cryogenically cooled CPW through-line, we can measure the noise temperature of the components following the LNA and derive the gain of the LNA. The cryogenic noise temperatures presented here have been corrected for this backend noise contribution, which is in the range 0.5-3 K, depending on the frequency.

As demonstrated in [9], a significant improvement of maximum frequency of oscillation f_{max} of the transistor is expected when device is cooled to 20 K. This improvement may cause instability of the transistor. Therefore, a DC bias sweep was performed for the last stage of the amplifier. The results are shown in Fig 3 and Fig 4. As can be seen no abrupt changes are seen in the DC curves suggesting a stable transistor operation.

In the s-parameter and noise measurements Vb1, Vb2 and Vb3 were tied together and Vb4 was biased separately. Cryogenic s-parameters were measured in several bias points and the results are shown in Fig 5 and Fig 6. As expected gain increases when bias voltage and therefore bias current is increased. The cryogenic small signal gain is improved around 2 to 3.5 dB per stage compared to the room temperature gain, which is expected due to the improvement of f_{max}.

Fig. 7 shows cryogenic noise and derived gain of the CMOS LNA for several bias points. The best result was obtained with Vb1, Vb2 and Vb3 set to 0.7 V (13.3 mA drain current) and Vb4 set to 0.9 V (13.8 mA drain current). The measured noise is between 108 to 155 K from 75 to 115 GHz. A second chip was measured and the results between two chips are compared in Fig 8. The measurement results between two chips show similar performance.

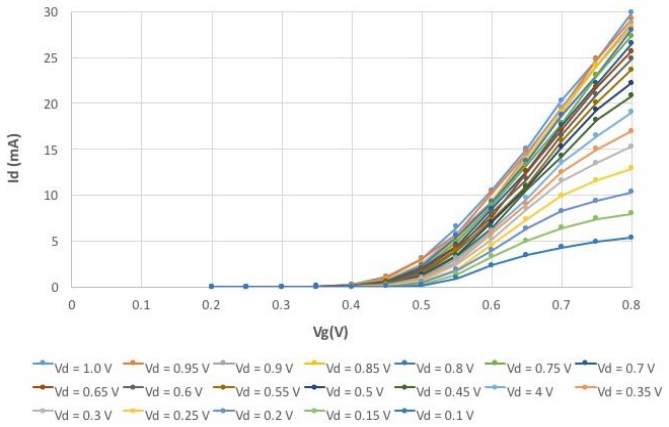

Fig. 3. Measured drain current of a transistor in function of Vgs for Vds voltages from 0.1 to 1 V in 0.05-V steps.

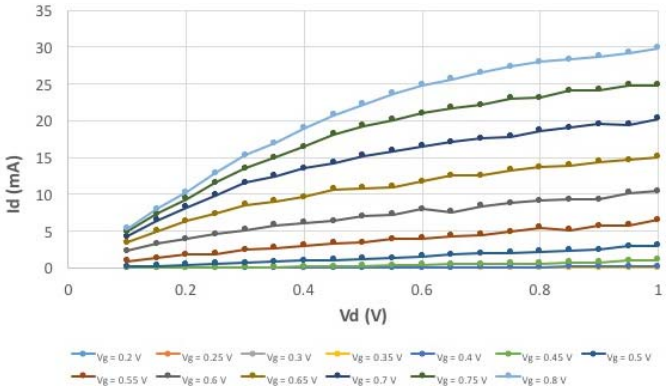

Fig. 4. Measured drain current of a transistor in function of Vds for Vgs voltages from 0.2 to 0.8 V in 0.05-V steps.

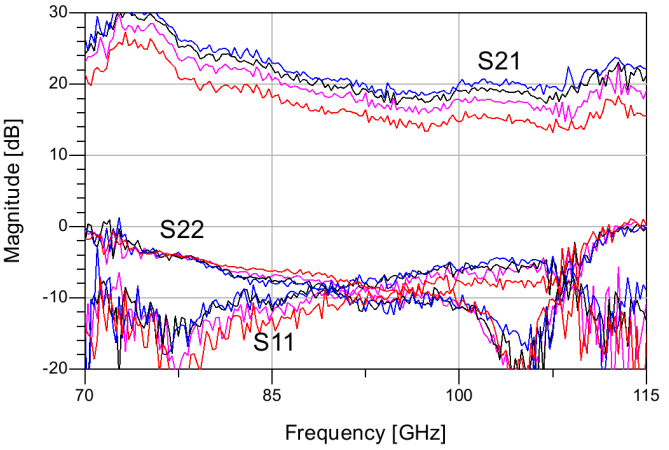

Fig. 5. Measured cryogenic s-parameters of the CMOS low-noise amplifier. Vb1, Vb2, and Vb3 are tied together and swept from 0.6 V to 0.75 V with 0.05-V steps. The corresponding total currents were 6.28 (red), 9.64 (pink), 13.3 (black) and 16.35 (blue) mA, respectively. Vb4 was fixed to 0.9 V with corresponding currents of 7.4, 10.5, 13.8 and 16.5 mA.

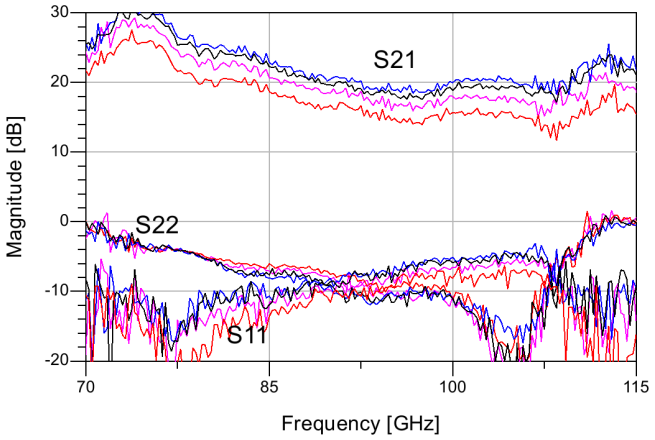

Fig. 6. Measured cryogenic s-parameters of the CMOS low-noise amplifier. Vb1, Vb2, and Vb3 are tied together and swept from 0.6 V to 0.75 V with 0.05-V steps. The corresponding total currents were 6.28 (red), 9.74 (pink), 12.75 (black) and 16.83 (blue) mA, respectively. Vb4 was fixed to 1 V with corresponding currents of 8, 11.3, 14.1 and 17.8 mA.

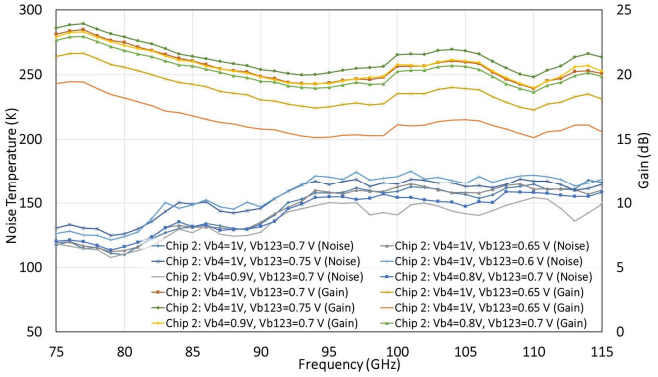

Fig. 7. Measured cryogenic (20 K) noise and gain of the CMOS low-noise amplifier for several bias points.

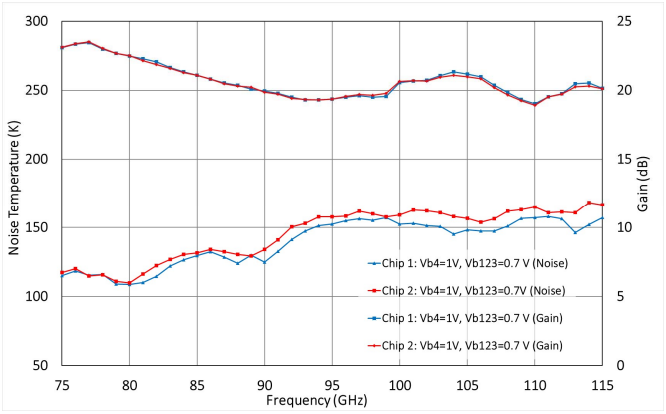

Fig. 8. Measured cryogenic (20 K) noise and gain of two CMOS low-noise amplifier chips.

TABLE I COMPARISON OF ROOM TEMPERATURE AND CRYOGENIC PERFORMANCE OF THE CMOS LOW-NOISE AMPLIFIER

Ambient	Freq [GHz]	Noise [K]	Gain [dB]	Gain/stage [dB]	P_{DC} [mW]
Room temp.	75-105	865	>12	4	38
Cryo (20 K)	75-115	108-155	19-23	6-7.5	22

IV. CONCLUSION

Cryogenic measurements of millimeter-wave CMOS amplifier were presented for the first time. The cryogenic measurement results are compared to room-temperature performance in Table 1. The CMOS amplifier achieved 108-155 K noise temperature from 75 to 115 GHz when cryogenically cooled to 20 K. This is around 6 to 8 times improvement over the room temperature noise. To the best of authors' knowledge these are the lowest noise temperatures reported for any silicon based amplifiers operating around this frequency range.

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