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Focused Review on Print-Patterned Contact Electrodes for Metal-Oxide Thin-Film Transistors

Fei Liu, Liam Gillan, Jaakko Leppäniemi, and Ari Alastalo*

Metal-oxide-semiconductor-based thin-film transistors (TFTs) are exploited in display backplanes and X-ray detectors fabricated by vacuum deposition and lithographic patterning. However, there is growing interest to use scalable printing technologies to lower the environmental impact and cost of processing. There have been substantial research efforts on oxide dielectric and semiconductor materials and their interfaces. Materials for the source/drain (S/D) contact electrodes and their interface to the semiconductor have received less attention, particularly concerning the usage of printing processes. Specific contact resistivity of oxide TFTs with print-patterned S/D contacts can be 10^{-2} to 10^{1} Ω cm^2, significantly higher than vacuum-deposited contacts around 10^{-5} to 10^{-3} Ω cm^2. Problems at the semiconductor/S/D interface, such as large contact resistance, poor adhesion, or cross-interface contact material migration, affect device characteristics causing hysteresis loops, kink or step-like distortion, and threshold voltage shift. This work reviews advances in materials and fabrication methods of print-patterned S/D electrodes for oxide TFTs. Differences in characterization methods among existing literature hamper comparing the performance of print-patterned S/D contacts. Therefore, systematic and standardized measurements are proposed to assist identification of possible problems, which to some degree can then be mitigated by device fabrication strategies, facilitating well-performing printed contact electrodes for metal-oxide TFTs.

1. Introduction

Thin-film transistors (TFTs) are key electronic components that are currently widely used and studied in the fields of flat-panel displays,[1–3] pixelated X-ray detector backplanes,[4–7] biosensors,[8,9] and integrated circuits.[10,11] TFTs based on metal-oxide semiconductors, such as indium gallium zinc oxide (IGZO),[12–17] have gained much attention due to their optical transparency, mechanical flexibility, higher charge-carrier mobility than that of organic materials or amorphous silicon, and low processing temperature as compared to amorphous and polycrystalline silicon TFTs.[18–21]

Parallel to the achievements of metal-oxide TFTs, organic materials, carbon nanotubes (CNTs), and 2D materials have also been constantly developed. For recent reviews, see refs. [22,23]. The material approaches differ in their characteristics such as charge-carrier type (electrons or holes), charge-carrier mobility, environmental and electrical stability, mechanical flexibility, operation voltage, thermal budget of processing, technology readiness level for high-throughput fabrication, and sustainability (environmental footprint of materials and processes). There are also approaches that combine different material classes, for example, to implement complementary logic by combining the predominantly n-type oxide TFTs with p-type organic TFTs.[24] In this paper, we focus on the metal-oxide TFTs that are among the highest-performing alternatives for flexible thin-film devices that can be patterned by printing and that have already reached the maturity of being used in product fabrication (e.g., flat-panel displays).[2]

The first metal-oxide-based TFT employed tin oxide (SnO_2) as the semiconductor and was invented by Klasens et al. in 1964, opening the door for research into transparent metal oxide TFTs.[25] Owing to the technology and material-processing limitations at that time, only a few studies focused on this area until 2003. During that year, zinc-oxide-based (ZnO) TFTs with mobility of $\mu = 2.5$ cm^2 V^{-1} s^{-1} were successfully manufactured by Hoffman et al., Carcia et al., and Masuda et al.[26–28] In the same year, Nomura et al. made a breakthrough with the first use of the quaternary-oxide semiconductor IGZO in a single-crystalline form to fabricate the TFTs, rather than some more conventional binary oxides such as ZnO, indium oxide (In_2O_3), and SnO_2. This kind of device that required annealing at 1400 °C displayed better electrical properties than its binary counterparts, with 80 cm^2 V^{-1} s^{-1} mobility and a 10^6 on/off ratio.[29] The following year in 2004, they reported flexible TFTs fabricated at room temperature on polymer film based on amorphous IGZO (a-IGZO) with saturation mobility of ≈6–9 cm^2 V^{-1} s^{-1}.[30] The discovery of a-IGZO raised substantial interest in research on amorphous metal-oxide TFTs and their low-temperature

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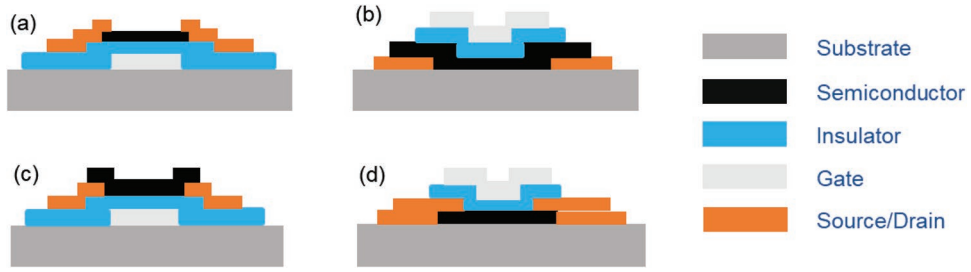

Figure 1. Side view of four major structures of TFTs. a) Bottom gate top contact (BGTC). b) Top gate bottom contact (TGBC). c) Bottom gate bottom contact (BGBC). d) Top-gate top contact (TGTC).

processing for thin-film-, large-area-, and flexible-electronics applications.

The basic TFT structures are presented in **Figure 1** to serve as an easy reference for the discussion that follows. The categories are classified according to the position of a gate electrode and source/drain (S/D) contact electrodes.[18] The selection of the structure to be used needs to take many influential parameters into consideration, such as the processing steps, processing temperatures of the different materials, and application of the device (e.g., whether the semiconductor needs to be functionalized for biosensing, or protected from exposure to the environment by the dielectric). The composition of each constituent (gate, insulator, semiconductor, S/D) of a TFT can employ various materials. The developments focus on the materials themselves and/or on their fabrication process to obtain good electrical performance of the device. Conductive doped silicon (Si) wafers are a high-quality and commercially available choice for the common gate that can also serve as the substrate, and when oxidized, as the gate insulator. Consequently, Si wafers have been employed in many publications related to metal oxide TFTs.[31–33] However, circuits based on TFTs need patterning of the gate and the gate dielectric layers. For the gate dielectric part, except for the most commonly used silicon oxide (SiO_2) with a dielectric constant of $\varepsilon = 3.9$, other oxide materials with higher dielectric constants (high-k), like aluminum oxide (Al_2O_3) ($\varepsilon = 9$),[12] hafnium oxide (HfO_2) ($\varepsilon = 25$),[34] yttrium oxide (YO_x) ($\varepsilon = 15$),[35] and zirconium oxide (ZrO_x) ($\varepsilon = 25$),[31] have also been employed as they will allow lowering of the operation voltage. In addition to the binary oxides and the quaternary oxide IGZO that were discussed above, ternary oxides, such as indium gallium oxide (IGO),[36] indium zinc oxide (IZO),[33,37] and zinc tin oxide (ZTO),[38] have also been actively used as semiconductor materials due to their good electrical performance.

Currently, product manufacturing based on metal-oxide TFTs mostly relies on traditional processes of the thin-film semiconductor industry such as sputtering, chemical vapor deposition (CVD), and atomic-layer deposition (ALD).[22] However, solution-based processes are an unstoppable trend that is being developed due to their potential to reduce the number of needed processing steps and thermal budget, to achieve a low-cost fabrication process with easy composition adjustments. Spin coating[13,33,37,38] and inkjet printing[14,39–41] are the most commonly used solution-based fabrication methods. Additive printing methods, such as inkjet, can help to conserve the use of materials compared to etching processes. Print processing also carries advantages including i) processing in ambient pressure and humidity; alleviating the need for advanced vacuum techniques, and ii) scalability; high throughput manufacture of large volumes of devices are possible including fabrication of large area electronics by sheet-to-sheet or roll-to-roll processes. This motivates not only the print-patterning of the active oxide materials of the TFT devices but also the printing of various materials for the contact electrodes. To this end, there have been significant advances in print processing of the different parts of oxide TFTs such as gate insulators[42] and semiconductors.[43]

Facilitating the development of thin-film electronics, methods to characterize the basic TFT figures of merit based on output- (I_d–V_d) and transfer-curve (I_d–V_g) measurements, such as the charge-carrier mobility (μ), subthreshold swing (SS), threshold voltage (V_t), turn-on voltage (V_{on}), and on-off ratio (I_{ON}/I_{OFF}), are well established and widely used in the literature (for definitions see refs.[18,44,45]). These basic parameters are illustrated in the output and transfer curves for an ideal TFT in **Figures 2**a,b, respectively, and in the transfer curve for a real solution-processed TFT that deviates from the ideal characteristics in Figure 2c. When measuring the curves by sweeping the source-drain or gate voltage in both directions, the curves can show hysteresis, as denoted in Figure 2c. A parameter V_{hyst} can be used to quantify the hysteresis by defining it as the maximum voltage deviation in the I–V curves between the forward and reverse V_g sweep. The hysteresis is typically an indication of mobile and/or trapped charges in the device structure and is often observed for solution-processed materials.

Contact characteristics have been studied and reviewed for vacuum-processed metal-oxide TFTs.[46–48] On the other hand, print-patterned S/D contacts for oxide TFTs are less broadly studied. In recent years, this question has received some attention as evidenced by the reports related to print-patterned S/D electrodes for oxide TFTs shown in **Table 1**. Although some of the recent reviews of solution-processable TFTs also pay attention to the S/D electrodes,[20] to our knowledge, a comprehensive review on the subject is missing that would be useful to facilitate directing future research. In this focused review paper, we explain the importance of well-performing S/D contact electrodes and overview different materials that may be print-patterned for use as contact electrodes with metal oxide TFTs. This work endeavors to assess the inherent advantages and limitations of the current state-of-the-art, with an emphasis on the interface between print-patterned contact and oxide semiconductor.

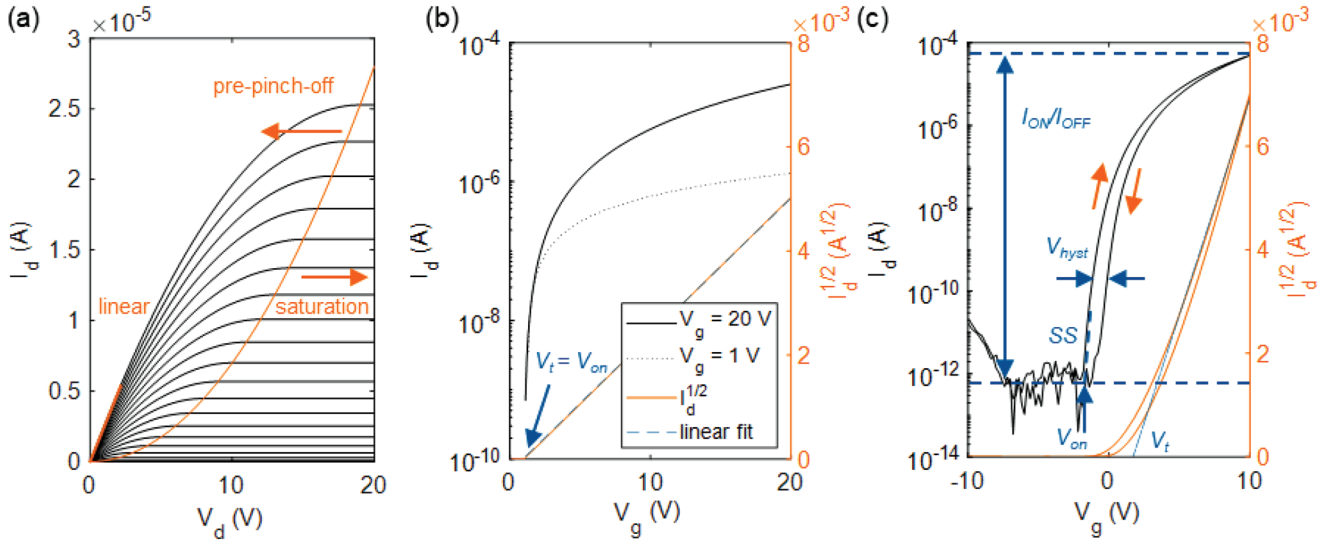

Figure 2. a) Output and b) transfer characteristics obtained from simulation using the ideal square-law model of TFT calculated using capacitance density for gate dielectric $C_i = 35$ nF cm^{-2}, $W/L = 2$, $\mu = 2$ cm^2 V s^{-1}, and threshold voltage $V_t = 1$ V, which equals V_{on} for ideal TFT. Different operation regimes are denoted in (a). c) Transfer curve data for a real TFT device (In_2O_3 TFT with ROP-patterned Al S/D-contacts) where current on-off ratio (I_{ON}/I_{OFF}), subthreshold slope (SS), hysteresis (V_{hyst}), turn-on voltage (V_{on}), and threshold-voltage ($V_t \neq V_{on}$) are denoted in the graph.

2. Characterization of Contact Electrodes for Oxide TFTs

In general, the contact should be a so-called silent partner of the TFT device and not limit its performance or lead to degradation, stability, or reliability issues over time. There are several simple methods to characterize the electrical performance of metal-semiconductor contact as discussed in the book by Schroeder.[84] Also, the publication by Hong et al. provides a good overview of the basic TFT equations, as well as issues arising from series resistance effects.[45] However, in the literature reporting printed or print-patterned contacts, those are typically not applied as a standard part of characterization, even when problems are observed. To help the reader to establish the use of these methods and form the basis for the latter discussion in this paper, in this chapter, we first discuss the important metrics and methods for characterizing S/D-contacts. Then, we focus on the potential issues arising from using printing or print-based patterning to form the S/D contacts as opposed to using conventional photolithography methods.

2.1. Contact Resistance and Metrics

The total resistance for a TFT with two contacts is given by

$$R_{total} = R_{ch} + 2R_c = r_{sh}\frac{L}{W} + 2R_c \quad (1)$$

where R_{ch} is the channel resistance and R_c is the contact resistance of one contact assuming that both contacts have the same contact resistance and neglecting effects that are assumed to be small such as probe wire resistance and probe-to-electrode contact resistance, or the electrode resistance. The channel resistance is further given as sheet resistance (r_{sh}) and the number of squares in the channel (L/W). The contact resistance is often multiplied by the channel width as $R_c \times W$ to allow comparison of devices with different geometries.

The contact effects can also be characterized by an experimentally-measurable quantity called specific contact resistivity ρ_c (also called specific contact resistance in some references) given in units of Ω cm^2 that lumps not only the effects posed by the S/D contact-semiconductor interface but also the areas above and below the interface.[84] Because ρ_c is independent of the contact area, it facilitates comparing dissimilar devices. The current flowing between the S/D contacts experiences both the sheet resistance of the channel r_{sh} (in the lateral direction in **Figure 3**a) and the specific contact resistivity ρ_c of the interface (in the vertical direction under the contact in Figure 3a). As the current finds a path of least resistance, depending on the contact size, only part of the contact area can be effectively taken part in the charge transfer between the S/D electrode and the semiconductor. This effective area can be described as $W \times L_T$, where L_T is the transfer length that is defined as[84]

$$L_T = \sqrt{\rho_c / r_{sh}} \quad (2)$$

For good contacts, the L_T should be small, typically at µm-level, to allow device miniaturization without an increase in contact resistance or current crowding that can lead to local Joule heating.[85] When the length of the contact is large enough, ≈>1.5 × L_T, such that the active area is not limited by the length of the contact, an approximate relation can be written between the contact resistance R_c and the specific contact resistivity,[84] where

$$R_c \approx \frac{\rho_c}{L_T W} \quad (3)$$

Table 1. Reported examples of metal oxide thin-film transistors with print-patterned source/drain contact electrodes.

Source/drain contact					Electrical performance				Contact performance	Ref.
Conductor type	Conductor	Semiconductor	Conductor deposition and patterning method	Conductor max. thermal treatment [min °C^{-1}]	W [µm]/L [µm]	μ [cm^2 V s^{-1}]	V_{on} [V]	V_{hyst} [V]	$R_c \times W/\rho_c/L_T/\rho_{S/D}$	
Printable metals	Ag	IZO	Dispensing printing	120/200	1000/280–450	7.9	5[a)]	–	–/–/–/7.6 µΩ cm	[33]
	Ag	IGZO	Inkjet printing	8/130	550/60–318	8.73	−2.5[a)]	–	8.18 kΩ cm/–/–/–	[12]
	Ag	In_2O_3	Inkjet printing	30/150	1200/80–300	3 ± 1.8	−5.2 ± 0.9	4 ± 0.7	3.48 ± 0.96 kΩ cm/24 ± 4 Ω cm^2/67 ± 5 µm/–	[49]
	Ag	IGZO	Inkjet printing	10/150	154/550	4.28	−2[a)]	–	1.2 kΩ cm[a)]/ 3.6 Ω cm^2[b)]/ 30 µm[a)]/–	[50]
	Ag	IGZO	Inkjet printing	–/–	551.29/31.09	0.29	0[a)]	–	–/–/–/–	[51]
	Ag	IGZO	Inkjet printing	30/200	300/60	0.071	−15[a)]	–	–/–/–/–	[52]
	Ag	ZTO	Screen printing	–	–/100	2.3	5	–	–/–/–/–	[38]
	Ag	In_2O_3	Inkjet printing	10/110	–/0.12	–	−5[a)]	–	–/–/–/–	[53]
	Ag	In_2O_3	Reverse offset printing	–/250	100–200/4–18	1.4 ± 0.4	−7.4 ± 1.6	2.5 ± 0.6	–/–/–/0.08 ± 0.04 Ω cm	[43]
	Ag	IGZO	Spray coating with shadow mask	–/120	300/300	4.75 ± 1.5	0[a)]	–	–/–/–/73.7 ± 36.1 µΩ cm	[54]
	Ag	IGZO	Non-relief lithography/ Dip-casting	30/180	40/5–20	0.05–0.2	−30[a)]	–	–/–/–/10^{-5} Ω cm	[55]
	Ag	ZTO	Electrohydrodynamic jet- printing	10/150	2750/420	0.97	4	10[a)]	–/–/–/4.05 µΩ cm	[56]
	Cu	ZTO	Reverse offset printing	10/250	1000/150	2.6	4[a)]	–	–/–/–/13 µΩ cm[a)]	[32]
	Cu	ZTO	Inkjet printing	60/200	3000/90	0.23	−5[a)]	–	92–2050 kΩ cm/–/– /1.29×10^7 µΩ cm	[57]
	Cu	IGZO	Screen printing with mesh mask	40/140	1000/90	2.06	0[a)]	–	–/–/–/–	[58]
	Cu	ZTO	Electrohydrodynamic jet- printing	45/300	950/95	0.5	3[a)]	–	–/–/–/0.1 ± 0.01. Ω cm	[59]
	Mo	IGZO	Screen printing	10/100	1000/100	13.5	0	–	–/–/–/35 µΩ cm	[60]
Printable conductive metal-oxides	ZIO	ZTO	Inkjet printing	30/600	1550/120	1.02	0[a)]	–	9–146 kΩ cm/–/–/ 0.4 Ω cm	[61]
	ATO	ZnO	Spray pyrolysis/ inkjet printing polymer patterning	–/350	308 ± 15/200 ± 3	30	–	–	–/–/–/0.015 Ω cm	[31]
	ATO	SnO_2	Inkjet printing	15/500	100/–	11	−2.5[a)]	–	–/–/–/0.04 Ω cm	[62]
	RuO	In_2O_3	Nanoimprinting (nanorheology printing and dry etching)	–/500	20/20	0.004	−1[a)]	–	–/–/–/3×10^{-4} Ω cm	[63]
	RuO_2	IZO	Rheology printing and Ar etching	–/350	28/0.5	12.9	0[a)]	–	–/–/–/–	[37]
	ITO	IGO	Nanoimprinting (nanorheology printing and dry etching)	–/450	20/20	0.08	−2.5[a)]	–	–/–/–/5×10^{-2} Ω cm	[63]
	ITO	In_2O_3	Rheology printing and Ar etching	–/500	28/0.5	10.2	−0.5[a)]	–	–/–/–/–	[37]
	ITO	ZIZO	Spin coating and physical dry etching	30/250	–/–	2.1	−2.5[a)]	–	–/–/–/4.2 × 10^{-4} Ω cm	[64]
	ITO	InScO	Inkjet printing	60/350	–/–	3.57	−3[a)]	≈0.1	–/–/–/–	[65]
	ITO	ITO	Inkjet printing	60/350	600/40	33.1 ± 2.4	−0.09	–	–/–/–/–	[66]
	ITO	ZTO	Inkjet printing	30/500	2000/180	0.16	0[a)]	–	–/–/–/0.02 ± 0.001 Ω cm	[67]
	ITO	ZnO	Inkjet printing	–/400	2000/150	135	1[a)]	≈1[a)]	–/–/–/–	[35]

Table 1. Continued.

Source/drain contact					Electrical performance				Contact performance	Ref.
Conductor type	Conductor	Semiconductor	Conductor deposition and patterning method	Conductor max. thermal treatment [min °C^{-1}]	W [µm]/L [µm]	μ [cm^2 V s^{-1}]	V_{on} [V]	V_{hyst} [V]	$R_c \times W/\rho_c/L_T/\rho_{S/D}$	
	ITO	In_2O_3	Inkjet printing	60/350	2.95 ± 0.35/ 3.5 ± 0.7	3.65 ± 1.25	−12.5[a)]	–	−/−/−/2.4 × 10^{-1} Ω cm	[68]
	ITO	IGZO	Photolithography and wet etching	−/−	−/−	7.6	0[a)]	–	1.17–64.1 kΩ cm/ −/−/−	[14]
	ITO	In_2O_3	Electrohydrodynamic jet-printing	90/350	120/12	117	−0.7[a)]	–	−/−/−/4.57 × 10^{-3} Ω cm	[69]
	ITO/IZO	IGZO	Inkjet printing	30/400	500/50–200	0.82	−10[a)]	–	2.5 kΩ cm/ 1.25 Ω cm[2b)]/ ≈5 µm[a)]/−	[39]
	AZO	ZnO	Inkjet printing	−/−	400/100	3	−2.5[a)]	–	−/−/−/−	[70]
	ACO	InO_x	Inkjet printing	160/250	−/−	19	−0.5 ± 0.25	<0.1	≈160 Ω cm/−/−/−	[71]
	ACO	InO_x	Inkjet printing	160/250	400/250	12 ± 1.6	−2[a)]	<0.05	−/−/−/−	[71,72]
	FTO	ZTO	Inkjet printing	10/300	75–105/10–50	0.04	4[a)]	–	−/−/−/0.4 Ω cm	[40]
	MoO_x	IGZO	Reverse Offset Printing	1/200	240/60	0.17	−8[a)]	–	−/−/−/10 mΩ cm	[13]
Printable carbon-based and other materials	Au/graphene	FA-IGZO	Transfer printing with stamping	−/−	1000/60	3.2	0[a)]	–	−/−/−/	[73]
	ITO/Au	IGO	Thermal evaporation/inkjet printing	60/350	50/<2	2.9	−0.5[a)]	–	−/−/−/3.9 × 10^{-5} Ω cm	[74]
	MWCNT/PSS	ZnO	Electrohydrodynamic jet printing	−/−	100/−	1.08 ± 0.39	−1[a)]	–	−/−/−/−	[75]
	Ti_3C_2	ZnO	Spray coating and lift off	30/175	250/100	2.61	−1[a)]	≈0.5	−/−/−/32 µΩ cm	[34]
	Ti_3C_2	SnO	Spray coating and lift off	30/175	100/100	2.01	10[a)]	≈3.3	−/−/−/−	[34]
	AgNWs/ PEDOT:PSS	ZnO	Spray coating with a shadow mask	10/80	1000/185	9.1	0[a)]	–	−/−/−/41.3 ± 1.4 µΩ cm	[76]
	SWCNT	In_2O_3	Spray coating with a shadow mask	−/115	1000/100	7.12 ± 0.43	0[a)]	≈0.2	−/−/−/2.2 mΩ cm	[77]
	SWCNT/AZO	In_2O_3	Spray coating/ spin coating with photolithography and lift off	−/115	1000/200	5.44	0.5[a)]	≈1[a)]	2.024–17.224 kΩ cm/ −/−/−	[78]
	Graphene	IGZO	Inkjet printing	20/300	250/−	6.42	3[a)]	≈5[a)]	2.9 ± 0.2kΩ cm/ 18 Ω cm[2b)]/ 62.5 µm[a)]/−	[41]
Vacuum-deposited print-patterned metals	H-doped a-IGZO	a-IGZO	Top gate by imprint lithography as mask for NH_3-plasma doping of a-IGZO	−/350	0.45	≈9	−1.6	–	−/−/−/−	[79]
	Al	In_2O_3	Reverse offset printing and lift off	10/100	−/−	1.4	−15[a)]	≈5[a)]	−/−/−/−	[80]
	Al	In_2O_3	Reverse offset printing and lift off	30/100	−/−	1.8 ± 0.3	−0.36 ± 0.13	0.89 ± 0.15	−/−/−/−	[81]
	Au	In_2O_3	Electron beam evaporation and chemical lift-off lithography	−/−	35/15	11.5 ± 1.3	−5[a)]	–	0.13 kΩ cm/0.065 Ω cm[2b)]/5 µm[a)]/−	[82]
	Cr/Au	In_2O_3	Electrohydrodynamic jet-printed etch resist	−/−	−/−	3.6	−20[a)]	–	−/−/−/−	[83]

[a)]Value estimated from figure inside reference paper; [b)]value calculated using values of other parameters using Equation (3).

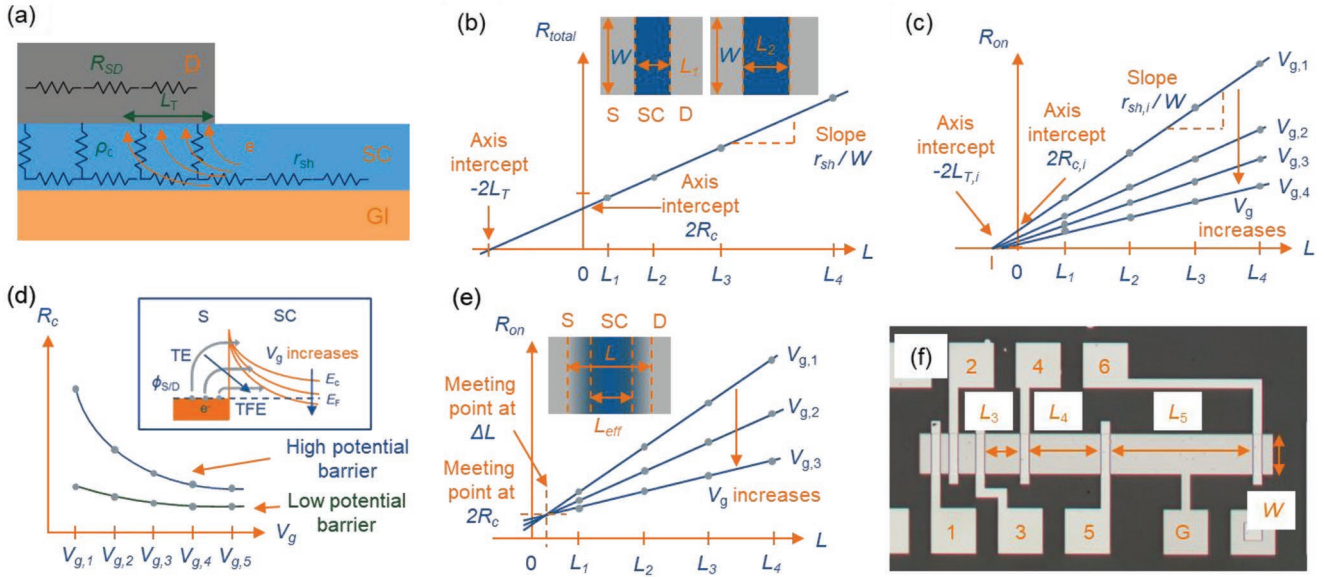

Figure 3. a) A schematic image of drain contact interface leading to the concept of transfer length L_T. b) A schematic graph for a TLM measurement of total resistance R_{total} as a function of inter-electrode distance L. Inset shows the relevant channel dimensions. c) A schematic graph for the gated-TLM measurement of total ON-state resistance $R_{total,on}$ as a function of inter-electrode distance L. Axis intercepts of each curve can be used to calculate the gate-dependent L_T, r_{sh}, and R_c values. d) Plotting R_c as a function of V_g for cases with high and low potential barriers. Inset shows a schematic image of barrier lowering at source contact with a high potential barrier where increasing V_g results in enhanced thermal field emission (TFE) besides thermal emission (TE) over the potential barrier. e) A schematic graph for a gated-TLM measurement for doped contact, where the family of curves crosses at a point that defines the ΔL and $2R_c$. Inset shows the concept of effective channel length L_{eff}. f) A microscope image of a gated-TLM test structure with six electrodes with increasing inter-electrode distance. *G* denotes the gate electrode to apply V_g while measuring the total resistance to get a family of TLM curves. The patterned transparent oxide semiconductor is not visible in the optical microscope image.

For long contacts, deviations of the actual length of current distribution at the contact from Equation (2) can occur for very thin semiconductor films or if the electrode resistivity is high.[85]

As a benchmark for print-patterned contacts in Table 1, contact characteristics of high-quality vacuum-processed TFTs have been widely studied.[86–94] For example, values as low as $\rho_c = 10^{-5}$–10^{-3} Ω cm^2 are reported in the literature for IGZO[16,17] and gallium oxide (Ga_2O_3),[47] but the reported range covers several orders of magnitude up to $\rho_c = 10$ Ω cm^2 depending on S/D material. Furthermore, $\rho_c < 10^{-4}$ Ω cm^2 were found for Ag, In, Ti, ITO, and amorphous IZO (a-IZO) S/D contacts for pulsed laser deposited a-IGZO TFTs, where Ti and ITO formed Ohmic contacts and resulted in better TFTs than devices with Au Schottky-contacts.[16] For R_cW, the values reported in the literature for IGZO TFTs with vacuum-deposited contact electrodes also have a wide range from ≈1 Ω cm to ≈10 kΩ cm depending on contact material, processing conditions, and operation point.

The contact resistance is often characterized using the transfer length method (TLM), where multiple contacts are deposited with increasing inter-electrode distance L over a slab of semiconductor with width W as shown in Figure 3b. By measuring the total resistance between the adjacent contacts (L_i) and plotting the resistance as a function of inter-electrode distance, based on Equations (1)–(3), we obtain

$$R_{total} = r_{sh}\frac{L}{W} + 2R_c \approx \frac{r_{sh}}{W}(L + 2L_T) \quad (4)$$

Then, as shown in Figure 3b, the r_{sh}/W, $2R_c$, and -2 L_T can be read from a line fit to the R_{total} versus L data as the slope, the R_{total}-axis intercept, and the L-axis intercept, respectively.

More complete information on the contact resistance can be obtained using a gated-TLM, where the total ON-state resistance, denoted as $R_{total,on}$ to highlight the difference to the conventional TLM described earlier, is measured at varied $V_g >> V_T$ in the linear regime ($V_d \to 0$) to obtain a family of TLM-curves.[95,96] The intercept points of the R_{on}-axis and L-axis, as well as the slope, are now dependent on the applied V_g and can be used to determine the R_c, L_T, and r_{sh}/W as a function of gate-voltage as shown in Figure 3c. Depending on the height of the potential barrier at the source-semiconductor interface, the R_c can have a large V_g dependence due to the gate-field-induced barrier-height and -width reduction that leads to enhanced thermal field emission (TFE) besides the thermionic emission (TE) over the potential barrier[55,97] as illustrated in Figure 3d.

S/D contacts with a heavily-doped interface region are formed when using oxygen-scavenging materials, like Al[98,99] or Ti,[100] as top-contacts on oxide semiconductors for which oxygen vacancies act as charge donors, such as IGZO or In_2O_3, or by the diffusion of dopants such as hydrogen to the channel.[79] Such contacts can also be characterized using gated-TLM. The family of curves meets at a point that defines both the $\Delta L = L - L_{eff}$, which indicates a shorter effective channel length (L_{eff}) than the channel dimensions (L) defined by the gap between the patterned S/D electrodes, and the approximate R_c as shown in Figure 3e.[84] An example of a gated-TLM-test structure with six electrodes is shown in Figure 3f.

Table 2. Summary of key TFT characteristics.

TFT characteristics		Measurement methods	Reported range in Table 1
Name	Acronym [unit]		
Mobility	μ [cm^2 V s^{-1}]	From transfer measurements. Different definitions are used such as saturation, field-effect, effective, incremental, and average mobility (see refs. [44,84]).	0.004–135
Turn-on voltage	V_{on} [V]	From transfer measurements.	−30–10
Hysteresis	V_{hyst} [V]	Back-and-forth output and transfer measurements.	0.05–5
Normalized contact resistance	R_cW [Ω cm]	TLM. Gated TLM to characterize as a function of gate voltage.	130–2.05 × 10^6
Transfer length	L_T [μm]	TLM. Gated TLM to characterize as a function of gate voltage.	5–72
Specific contact resistivity	ρ_c [Ω cm^2]	Calculated using L_T, r_{sh}, R_c, and W as shown in Equations (2)–(3)	0.065–28
Electrode resistivity	$\rho_{S/D}$ [μΩ cm]	Four-point measurements	7.6–1.29 × 10^7

Besides the TLM and gated-TLM discussed here, various other methods have been developed for determining the R_c in MOSFETs, such as the cross-bridge Kelvin resistance (CBKR), Kelvin probe force microscopy (KPFM), and TLM, based on circular test structures as discussed in the book by Schroder[84] and in ref. [94]. Those should be equally applicable for characterizing print-based contacts for oxide semiconductors.

TFT characteristics with print-patterned S/D electrodes reported in the literature that are collected in Table 1 are summarized in **Table 2** along with the relevant measurement methods. Comparing to the above-discussed benchmark values of vacuum-processed high-quality TFTs with contact characteristics $\rho_c < 10^{-4}$ Ω cm^2 and $R_cW \approx 1$ Ω cm, the best values in Table 2 are ≈100 times higher or more, highlighting the room for improvement in print-patterned contacts.

2.2. Challenges in Printed and Print-Patterned Electrodes

The interface between the metal contact and the semiconductor plays a major role in what constitutes a good contact. When the contacts are deposited using printing in ambient conditions as opposed to conventional photolithography and vacuum deposition performed in controlled conditions, several problems can occur and be observed from the basic transfer and output characteristics, as illustrated via schematic images in **Figure 4**. It should be noted that similar deviations from the ideal TFT characteristics can also originate from semiconductor, gate dielectric, or their interface, and thus, the cause of the problem cannot always be pinpointed without detailed electrical and complementary chemical or morphological characterization. Methods combining print-based patterning and vacuum deposition are less susceptible to some of the problems, which are also discussed later.

In general, contacts can be divided qualitatively into linear/Ohmic or non-linear/Schottky-type, where linear/Ohmic contacts are able to supply current without severely limiting the device performance, whereas non-linear/Schottky-contacts have rectifying I–V characteristics. Schottky-contacts can be utilized for low-power operation at a deep subthreshold region near the OFF-state.[46] Low-power means these devices might not experience Joule heating to an extent that could be incompatible with thermally sensitive materials such as flexible polymer substrates. However, Schottky contacts can lead to problems such as signal distortion when operating at ON-state in the linear regime with low V_d conditions where non-linear I–V with upward curvature can be observed in the output curve (see Figure 4e). Similar characteristics with upward curvature at low V_d can also arise from current crowding effects, especially for devices with staggered contacts (bottom gate top contact [BGTC] in Figure 1a or top gate bottom contact [TGBC] in Figure 1b) where the charge carriers need to flow from the S/D electrodes through a space-charge region to the channel at the semiconductor-dielectric interface.[101,102] The absence of such effects can be observed when taking the derivative of the output curves, that is, $\partial I_d/\partial V_d$, which should appear nearly constant in the low V_d range.[103,104]

Although in a simple Schottky-barrier model, selecting an S/D metal with a lower work function (WF, $\varphi_{S/D}$), than that of an n-type semiconductor would lead to a contact with accumulation interface and no barrier, controlling the contact type in practice is not as straightforward. Due to Fermi level pinning, a depletion interface with nearly constant barrier height can be formed regardless of the $\varphi_{S/D}$. However, the width of the formed barrier can be tuned by controlling the doping level in the semiconductor and thus enhance the tunneling of electrons from the metal to the semiconductor by TFE.[84] In this case, a Schottky-contact would have a high V_g-dependence of R_c[55,97] as shown in Figure 3d. For very high doping concentrations, field emission (FE) can be the dominant tunneling mechanism favoring an Ohmic contact. The selection of the nanoparticle (NP) capping agent of a metal ink and the annealing conditions have been shown to affect the $\varphi_{S/D}$ and lead to a reduced R_c.[57] One strategy that was already mentioned above to induce doping in the oxide semiconductor near the vicinity of the contact interface is to use print-patterned and vacuum-deposited contact metals that are self-passivating and lead to oxygen vacancy generation in the semiconductor, for example, Al and Ti, that have higher Gibbs free energies of oxidation than the semiconductor.[57,58,61] By scavenging oxygen, a compound interface with thin nm-level interface oxide can form that allows efficient field emission thanks to the local high doping density in the oxygen-deficient oxide semiconductor, thus resembling the n^+n-junction contacts in conventional Si MOSFETs.

A large resistance in series with the channel, such as a high-resistivity S/D electrode material ($\rho_{S/D}$) or a large contact resistance R_c, affects the performance of the TFT as only part of the voltage drop that is externally set between the source and drain

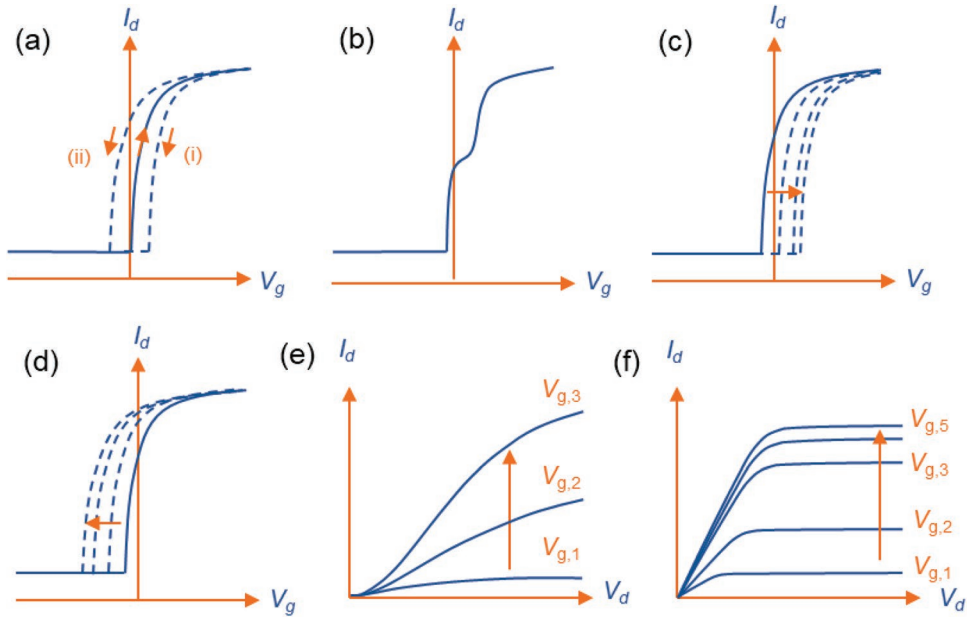

Figure 4. Schematic images of some non-idealities in TFT transfer and output curve. a) Transfer curve measured forward and backward leading to i) clockwise or ii) anti-clockwise hysteresis loop. b) Kink or step-like distortion in the transfer curve. c) Threshold voltage shift in positive V_g-direction between successive measurements. d) Threshold voltage shift in negative V_g-direction. e) Upward curvature in the low-V_d region of the output curve (Schottky-contact or current crowding). f) Output-curve with the contact-resistance-limited operation.

terminals (V_d) occurs over the channel. This will both limit the current drive capability (effectively decreasing the mobility) and shift the pinch-off condition toward more positive values by $V_{d,\,sat} = V_g - V_{ON} + I_D R_c$.[45] High parasitic resistances will also limit high-frequency TFT characteristics due to longer resistor–capacitor time constants. For S/D-contacts based on printed metal NPs, optimizing the sintering method and process conditions can help to minimize $\rho_{S/D}$.[105] Also, controlling the doping of the conductive polymers, such as PEDOT:polystyrene sulfonate (PSS), can be used to decrease $\rho_{S/D}$. However, such materials with conductances of ≈1000 S cm^{-1} at most[106] are typically not conductive enough to be used in S/D wiring. If the R_c limits the device performance, based on Equations (2) and (3), increasing the contact width (W) or decreasing the channel sheet resistance r_{sh}, for example, by doping could be used in applications where high device density is not critical.

As already mentioned above, when the potential over the oxide TFT is cycled back-and-forth in a transfer or output measurement, a hysteresis loop (V_{hyst}) (Figure 4a) can appear between the I_d of the forward and reverse sweeps. This signals that the active charge carrier concentration varies by the direction and history of the potential sweep and leads to alternating V_{on} and V_t. Also, step-like features, kinks, or humps can appear in the transfer curve (Figure 4b).[44,45,107–109] Such phenomena are typically associated with mobile ions or charge traps (donor or acceptor) residing at the semiconductor (e.g., impurities from unconverted precursors or grain boundaries), semiconductor-gate dielectric interface (e.g., dangling bonds or unoccupied traps in gate dielectric),[18] or in the case of non-encapsulated, bottom-gated devices, adsorbed molecules in the semiconductor (e.g., H_2O).[109] Besides these, the S/D-semiconductor interface can contribute to charge trapping. For example, the capping agent of the printed metal NPs can migrate to the S/D-semiconductor interface during sintering.[49] It has therefore been suggested that the selection of the capping agent of Ag NPs can affect the interface properties.[33,57] In addition, if the top interface of the oxide of a bottom-gate device is contaminated with adsorbed molecules prior to the contact deposition, those could remain in the pores of the printed S/D contact deposited at ambient conditions and contribute to the charge-trapping. To alleviate this problem, interface cleaning can be performed prior to the S/D-contact deposition either by an additional annealing or cleaning (solvent, plasma, etc.) step. Repeated measurements for an unstable device can lead to a V_t shift in the positive (Figure 4c) or negative (Figure 4d) direction in the V_g-axis of the transfer curve, depending on the origin and location of the traps and/or mobile ions.[110–112] Furthermore, the mobile charges in the gate dielectric can lead to electric double-layer effects that can strongly enhance low-frequency gate capacitance. Consequently, if the gate capacitance to be used in the DC current equations is determined from high-frequency measurements (often measured at 1 kHz), there is a risk to overestimate the charge-carrier mobility.[113,114]

Depending on the materials of the S/D electrodes, oxide semiconductor, and the deposition method, migration of contact electrode metal ions, oxygen, oxygen vacancies, as well as extrinsic dopants (e.g., H), can occur at the S/D-semiconductor interface. For example, Ag has been reported to migrate to oxide semiconductors from inks during thermal treatments or during electrical stress, which can lead to shorted devices, hysteresis, and long-term stability problems although initially the contact can be improved by enhanced field emission.[33,43] By controlling the Ag NP capping agent composition and annealing conditions, one can limit the migration.[33,57] Also the oxygen originating from the semiconductor can lead to oxidation of the deposited contact metal resulting in charge traps.[43]

One possibility might be to use a thin interface layer at the S/D-semiconductor interface to block the migration, similar to the diffusion barriers used in integrated circuits.[115]

Adhesion is another interfacial phenomenon that contributes to contact performance. Interfaces can be qualitatively described as abrupt, compound, diffusion, or mechanically anchored as categorized, for example, by Ohring.[116] In the abrupt interface, the materials at the metal-semiconductor interface are only weakly interacting and clearly confined to separate regions, thus leading to interfaces with high stress, low diffusion, and adhesion. In the compound interface, the chemical reactions between the metal electrode and the semiconductor atoms lead to a thin interface region formed from the metal and oxygen originating from the metal oxide. This is a typical case for reactive metal films, such as Al or Ti, deposited on oxides. In the diffusion interface, a gradual composition change between the metal electrode and the oxide semiconductor is formed through the diffusion of metal atoms, originating from the electrode or the semiconductor, and/or oxygen. The degree of diffusion depends on the solubility, size of the diffusing ion (e.g., hydrogen or oxygen being smaller than metal ions), and availability and energetics of the vacancy sites in the host lattice. The type of formed interfacial oxides can be roughly characterized using a "Pilling–Bedworth ratio," which is calculated as the ratio of the molar volume of oxide to the molar volume of metal.[117] Finally, the mechanically anchored interface is formed when the surfaces are rough and allow mechanical interlocking that leads to high adhesion.

Although the role of adhesion in contact resistance cannot be clearly defined, a good S/D contact requires good adhesion. It is well known that for obtaining low $\rho_{S/D}$ for vacuum-deposited metal films, the adhesion should be adequate to avoid situations where cohesion energy surpasses adhesion and leads to aggregation[118] or where hillocks are formed during electrical stress.[119] Especially for printed contacts on oxide semiconductors, the adhesion cannot be overlooked, as the print-deposition of NPs, such as Ag or Cu, on top of an atomically smooth oxide is more likely to lead to abrupt interface with poor adhesion and point-like contact between the metal and the oxide film. Poor adhesion could have a drastic impact on the long-term stability and mechanical durability of the TFTs. Surface treatments that roughen the oxide surface are one way to improve the adhesion but can lead to an increase of charge scattering at the interface. Other options include adding a thin sticking layer at the interface that promotes good adhesion.[49]

Finally, with respect to materials, the printed S/D-contacts formed from sintered metal NP inks tend to be porous even after sintering,[12] whereas vacuum-deposited and print-patterned thin-films are more bulk-like. In a porous interface, the current is forced to flow through the areas where the metal is in close contact with the semiconductor, which can increase the effective L_T and also lead to large local current densities, which can, for example, lead to electromigration-induced long-term stability problems. By controlling the sintering conditions, the grain growth of the NPs can be enhanced to obtain a larger effective contact area.[105]

In terms of processing accuracy, high resolution and good alignment control are important for high-quality contacts, as well as for device performance, in general. Resolution in terms of minimum line width and line spacing, as well as edge definition, sets the limit for device miniaturization and together with accurate alignment of consecutively fabricated layers helps to minimize parasitic capacitances caused by the gate and S/D overlap. Poor overlay alignment can lead to poorly-controlled overlap areas between the S/D and semiconductor (or gate), which can lead to a large discrepancy between the areas of the S-SC and D-SC contacts. In such a situation, a large contact resistance could lead to output-curves where the increase in I_d is becoming limited for increasing V_g values (see Figure 4f) due to the small contact area.

The non-idealities and their possible mitigation pathways discussed above are summarized in **Table 3**. Print-based processing is discussed more in the next section.

3. Progress of Print-Patterned Source/Drain Contact Electrodes

Patterning of contact electrode material for oxide TFTs can be achieved through various printing processes. This chapter first introduces frequently used printing methods, and then overviews recently reported strategies for the printing of i) metal, ii) metal oxide, iii) carbon-based or other materials, as well as iv) print-patterning of vacuum-deposited thin-films as S/D contacts for oxide TFTs. After that, **Table 4** summarizes key aspects of the processes and materials that are relevant for oxide TFTs.

3.1. Printing Methods

Figure 5a–f depicts several printing and coating methods that are commonly employed for the patterned deposition of materials to be used as source/drain electrodes for TFTs. These processes are described in the following paragraphs along with their inherent benefits and limitations, and can be grouped as either contact (e.g., screen printing, reverse offset printing [ROP], gravure printing, and flexography printing) or non-contact (e.g., inkjet printing and spray coating) methods.[120,121] Figure 5g presents film thickness and print resolution capabilities of different methods, which are critical parameters for the fabrication of thin-film electronic components. It should be noted that dispensing and slot die coating are not typically used for print-patterning of S/D contact materials for TFTs, in part due to their poor spatial resolution as compared to the other printing methods (Figure 5g). Besides the printing resolution and film thickness, overlay accuracy is also of utmost importance for printed multilayer devices, such as TFTs, to avoid poor yield, large contact resistances, and parasitic capacitances.

Inkjet printing operates by either thermal or piezoelectric ejection of picolitre-size ink droplets from a nozzle onto an underlying substrate (Figure 5a-i.[123] This digital direct writing process minimizes ink wastage and benefits from adaptable patterning, with designs tailored quickly using the software. However, inkjet printing has a lower throughput than the contact printing methods because of the need to raster the print head across the substrate.[124] The selection of inkjet-printable inks is limited by viscosity to about <20 mPa s, and it is recommended that solutes should be smaller than about 1/20 of the

Table 3. Non-idealities in oxide TFT performance arising from print-patterned contacts, their implications, and possible ways to avoid the problems.

	Issues arising from printed S/D-SC contact	Impact on the electrical characteristics	Implications to the device operation	Possible ways to avoid	Ref.
Process related	Poor printing resolution with a large channel length (L)	Low I_d due to large channel resistance, low operation frequency	Large devices lead to low yield and large variation	Utilize high-resolution printing methods such as reverse offset printing.	–
	Poor alignment accuracy between gate, semiconductor, and S/D.	High series resistance due to misaligning or high parasitic capacitances	Low yield, large variation, or compromised high-frequency operation.	Utilize high-accuracy alignment control or self-aligned processes.	–
Material related	Schottky-contact interface	Upward curvature in output curve at low V_d	Unreliable/hindered operation in the linear regime, power consumption	Apply interface engineering by material selection	[16,84]
	Large resistivity of S/D material ($\rho_{S/D}$)	Apparent decrease in μ at large V_g, $V_{d,sat}$ shifts up by I_dR_c, increased L_T	Lower current drive capability at high V_g, compromised high-frequency operation, current crowding.	Tuning annealing/sintering conditions or SC doping level	[57,58,61,105]
	Large contact resistance (R_c)	Apparent decrease in μ at large V_g and $V_{d,sat}$ shifts up by I_dR_c	Lower current drive capability at high V_g, compromised high-frequency operation.	Use larger contact width (W) or smaller SC resistance (r_{sh})	[45]
	Traps at the S/D-SC interface and mobile charge in layers	Hysteresis loop in the transfer curve, kink or step-like features in the transfer curve, and V_t/V_{on} shift	Unstable device, can affect circuit performance, and overestimation of mobility can occur if not taken into account.	Apply interface cleaning or choice of materials	[18,34,43–45,107–112]
	Migration of S/D material to SC layer	Shorted devices, V_{on} shift, hysteresis, long-term stability problems	Unstable device, large variation	Apply a blocking interface or suitable NP capping agent	[33,57,115]
	Poor adhesion of S/D material	Long-term stability problems	Reliability problems, large variation	Apply surface roughening or "sticking layer"	[49,118]
	Porous S/D-SC interface	Reduced contact area leading to high local current density and increased L_T	Reliability problems, poor tolerance of high current densities	Tuning annealing/sintering conditions or material selection	[12,105]

nozzle diameter to avoid clogging.[125] Wetting interactions can be challenging to control due to the low ink viscosity, leading to discrepancies between the print layout design and the resulting patterned features. In addition, inkjet can suffer from the coffee ring effect, which is caused by differences in solvent evaporation rate between the center and edge of a printed feature.[126]

Jet printing technologies have been developed to reach resolutions below 10 µm and in some cases even below 1 µm by reducing the size of individually ejected ink droplets via a combination of small and sharp nozzles and the use of electrostatic or electrokinetic forces to draw the ink from the nozzle and guide it to the substrate. These high-resolution methods include electrohydrodynamic (EHD) jet printing,[127] super inkjet,[128] and electrostatic jetting (ESJET).[129] For example, EHD jet printing achieves line widths down to 0.7 µm.[130] A recent review article on jet printing of oxide TFTs states that the low viscosity ink of inorganic precursors makes jet printing-based methods an appropriate choice for the printing of inorganic materials.[131] However, a disadvantage of EHD jet printing is that the printed droplets can possess a charge that might have undesirable consequences on print resolution or device performance, for instance, when printing onto layers such as the gate dielectric or semiconductor.[130]

Spray coating of films is achieved when an atomizer produces fine droplets of precursor material that are transported by the carrier gas and gravity to the deposition site (Figure 5a-ii. Similarly, as in the EHD jet, an electrostatic field can be applied to the substrate, causing charged droplets to aggregate and form a film.[121] This method for large-area deposition can enable the patterning of features through a mask and has the benefit of facile material doping and multicomponent film generation by multiple passes,[132] enabling controlled thickness around 1 µm.[124] Limitations of spray coating are that the small droplet size means that long processing times are required to fabricate films of sufficient thickness, and it is only possible to use low-viscosity precursor materials.

In screen printing (Figure 5a-iii), a flood bar spreads ink across a mesh screen and then a squeegee is used to transfer the ink through patterned openings in the screen onto the underlying substrate. Screen printing can enable 100-µm thick films, which is desirable for electrical conductivity, but films can suffer from high roughness and the fabrication of thin films can be challenging because the inks are viscous (500–5000 cp).[124] Screen printing is widely used in industry (e.g., back and front contacts in Si photovoltaic cells, conductive tracks, and antennas) and it enables high-throughput fabrication either as a sheet-to-sheet or roll-to-roll (rotary screen) implementation.

Gravure printing (Figure 5a-iv) is performed using a metal plate or cylinder, the surface of which is patterned with recesses (cups) corresponding to the print pattern that transfers the ink to the target substrate (direct gravure). The recesses are filled with ink, after which a blade scrapes off the excess amount of the ink so that the raised portions of the cylinder become free

Table 4. Summary of processing and materials approaches for metal-oxide TFT contacts. For more details, see Table 1.

Processing	Process type	Examples	Pros	Cons
	Printing used for deposition and patterning at the same time.	Inkjet, screen, flexo, gravure, reverse offset.	Possible to achieve a simple process with low energy and material consumption.	Ink and surface chemistry must be optimized to avoid wetting problems such as coffee ring (can also be used as a benefit), limited material availability as inks, and porous structure, especially for NP inks. Annealing at high temperatures is needed to enable good conductivity and contact properties that can lead to the migration of contact material.
	Print-patterned uniformly deposited material	Evaporation, sputtering, or ALD combined with printing of lift-off resist, etch resist or SAM layer, etchant ink, growth inhibitor or area-selective doping	Bulk-like high-performance materials (also with low work function) can be used, good pattern definition and uniform film thickness.	More processing steps than with direct printing, materials waste unless circulated, difficult to fabricate thick layers.
Materials	S/D material type	Availability for printed electronics	Pros	Cons that need special attention (see text)
	Solution processable metal	Majority of commercial inks are for Ag (NP, NW, flake, salt-based) for various printing methods. Cu and Au NP inks also available.	High conductivity compared to other printed materials, Cu inks becoming more available (cost, sustainability).	Ag environmentally not desirable and of high cost, Cu needs an inert atmosphere or special annealing, contact resistance, and Schottky barrier, especially for Ag, poor adhesion of Ag, hysteresis, diffusion into SC, solvent, and capping residues.
	Print patternable vacuum-deposited metal	Wide selection of materials, also low-work-function metals such as Al.	Good Ohmic contact, low contact resistance, bulk-like conductivity possibility to use bilayer metals (e.g. Ti/Au), and possibly less migration to semiconductor when avoiding the annealing step.	Vacuum processing can cause changes in underlying layers.
	Metal oxide	NP and precursor inks, vacuum deposition, ITO, ACO, IZO.	Ohmic contact, low contact resistance.	Lower conductivity than for metal, high annealing temperature can harm other layers or cause migration.
	Other	Carbon, carbon nanotubes, graphene, and their composites with oxides, metals or conducting polymers, Titanium carbide, AgNW+PEDOT:PSS	Low cost and low processing temperature of carbon inks that are abundant, flexible, and chemically stable	Contact resistance and Schottky barrier (composite approach can help)

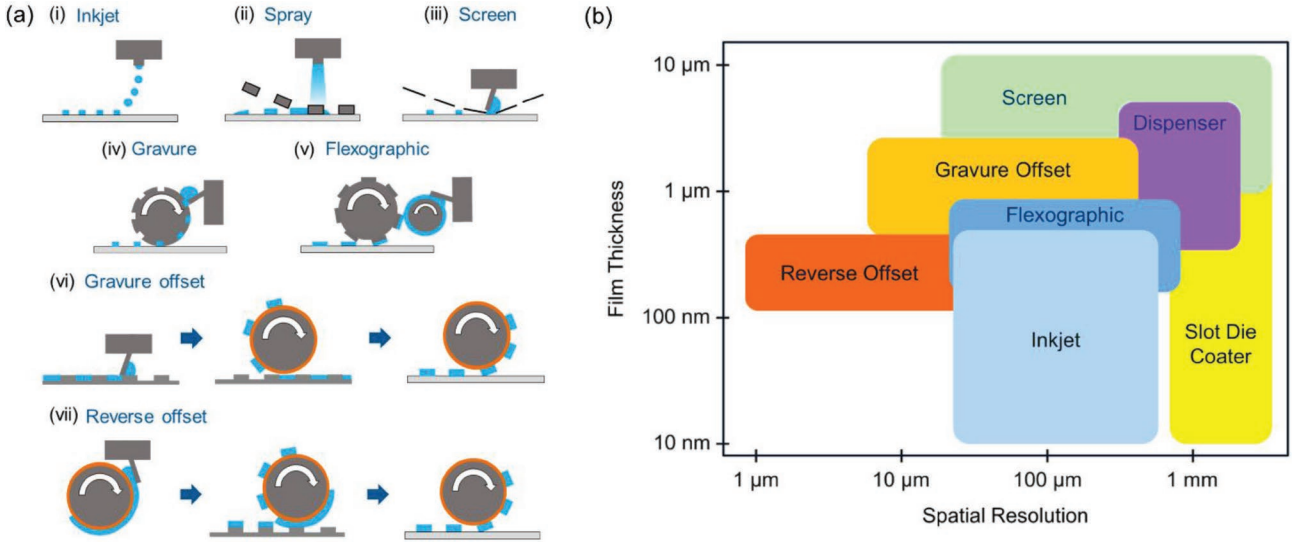

Figure 5. Schematic illustrations of some different print-patterning methods resulting in patterned deposition of blue-colored material by a) i) inkjet printing, ii) spray coating, iii) flat-bed screen printing, iv) rotary gravure printing, v) flexographic printing, vi) flat-bed gravure offset printing, and vii) flat-bed reverse offset printing. b) Thickness and resolution capabilities of films patterned by different printing methods. Reproduced with permission.[122] Copyright 2019, Elsevier.

of ink. The cylinder is then pressed against the target substrate to transfer the ink.[133] A disadvantage is that the pattern is defined by relatively high-cost cylinders, which do not allow rapid changes to print designs.[134] Flexographic printing relies on low-cost printing cylinders with flexible polymers that have raised patterns that are inked for the transfer of desired designs onto the substrate (Figure 5a-v).[134] Contact roller printing methods, such as gravure and flexographic printing, can enable more rapid printing speeds (>10 m s^{-1}) than non-contact methods such as inkjet or spray coating.[120,135] However, both in gravure and flexography printing, the ink is supplied to the substrate in separated spots that need to form a continuous structure through wetting, which can lead to thickness variations and splitting.[136]

Several methods are developed for high-resolution offset printing that uses printing or coating on an intermediate substrate (such as polydimethylsiloxane [PDMS]) followed by partial drying, a possible patterning step (in case of ink being coated onto the PDMS) and finally, transfers to the target substrate avoiding wet-ink–substrate-surface interactions such as line widening or coffee-ring effect. These methods include, in particular, gravure offset (Figure 5a-vi),[137] screen offset,[138] and ROP (Figure 5a-vii).[139] In gravure (screen) offset, gravure (screen) printing is used to define the print pattern on the PDMS intermediate substrate while in ROP, the PDMS substrate is uniformly coated with ink. In more detail, ROP is a three-step printing process as shown in Figure 5a-vii. First, an ink is uniformly coated onto a blanket (typically PDMS) and let to partially dry on the blanket. The drying alleviates ink spreading or deformation in the subsequent patterning step, where a cliché plate with elevated patterns is used to selectively remove regions of the ink from the blanket. Finally, the patterned ink is transferred from the blanket to the substrate.[139,122] The patterning of a partially dry film enables ROP to achieve micron-level print resolution (minimum line width/line spacing), uniform film thickness, and good line edge fidelity with a low taper angle,[80] which is highly beneficial for high-performance miniaturized TFT fabrication. A micron-level alignment accuracy is also possible with ROP.[13,140] ROP ink needs to have low viscosity (typically around 1–10 mPa s) and low surface tension for effective wetting of the PDMS blanket.[122,139] ROP can be implemented both as a sheet-to-sheet process using a planar cliché and as a roll-to-roll process using a cliché roll.[141] ROP achieves the highest accuracy in terms of linewidth, line space, thickness uniformity, line edge roughness, and alignment control among high-throughput printing methods as illustrated in Figure 5b. Some challenges in ROP include a lower throughput compared to the other contact printing methods (typical printing speeds <50 mm s^{-1}) and a limited maximum thickness (typically below 1 µm) due to a cohesive failure in too thick films that cannot reach the semidry condition throughout the thickness.

Sub 5-µm resolution has also been achieved for gravure printing with a printing plate fabricated using silicon microfabrication techniques. In that method, the printing plate is first fabricated on silicon using photolithography and etching, then it is replicated on metal by electroplating on UV-curable polyurethane acrylate negative mold. Using commercial inks and detailed modeling of the processing steps of cup filling, doctor blading, ink transfer, and ink spreading, 2 µm lines at a printing speed of 1 m s^{-1} are demonstrated.[142,143] Microfabrication techniques have also been used to make sub-10-µm-resolution flexographic printing plates on PDMS[144] or as polymer-coated CNT forests on a silicon wafer.[145]

Further high-resolution printing techniques include microcontact printing[146,147] where a patterned stamp is used to transfer the ink to the substrate. Typically, an elastomeric patterned stamp made of PDMS is used to receive the ink and transfer it to the substrate. The patterning of the stamp can be for example by surface height profile, that is, relief patterned PDMS (conventional microcontact printing),[148] by molecular functionalization of the surface (affinity microcontact printing),[149] or by adhesion contrast created by selective UV light exposure (adhesion contrast planography).[150] The coating of the stamp with ink can be performed by immersing the stamp in the ink (bath coating), or by contacting the relief patterned PDMS with another PMDS blanket that is uniformly coated with the ink.[147] Linewidths down to ≈0.1 µm have been demonstrated for conventional microcontact printing, which is mostly used to print thiols as a wet etch mask for vacuum-deposited Au layers.[147] However, solvent absorption into the relief patterned PDMS stamp can lead to PDMS swelling and printing defects, as well as challenges in overlay accuracy, especially with conventional microcontact printing.[147,151]

3.2. Materials

3.2.1. Printable Metals

High electrical conductivity along with often good mechanical and chemical robustness renders metals appealing materials for use as contact electrodes. However, the properties of bulk metals or even those of uniform thin-films deposited with vacuum-processes are challenging to reproduce in directly print-patterned structures. For instance, printable metal inks are commonly NP-based, which can result in a material that is composed of necked but discrete granular segments that can suffer from charge traps and mechanical instabilities. Nevertheless, a significant amount of research effort has been expended over recent years to develop strategies for realizing print-patterned metal contact electrodes using NP-based inks.

Copper (Cu) is naturally abundant, resulting in a lower cost than using more scarce metals such as silver (Ag) or gold (Au). The relatively low cost of Cu is a benefit for large-scale manufacture. Unfortunately, the susceptibility of Cu NPs to oxidation means that processing of these inks often demands an inert atmosphere.[152] Specialized photonic sintering equipment[153] can enable certain CuO_x-based NP inks to be processed in the air by reduction of the CuO_x to Cu.[154–157] Photonic sintering processes are known to be suitable for the fabrication of Cu contacts on oxide TFTs,[158] although careful consideration must be given to the thermal effects of the curing process on underlying materials such as semiconductors beneath the contacts.[159] A common strategy to alleviate the oxidation of Cu NPs is to use capping agents for the fabrication of shell-type NPs.[160–162] A seminal report of print-patterned Cu contacts for oxide TFTs relied on inkjet-printing and vacuum annealing of Cu NPs.[57]

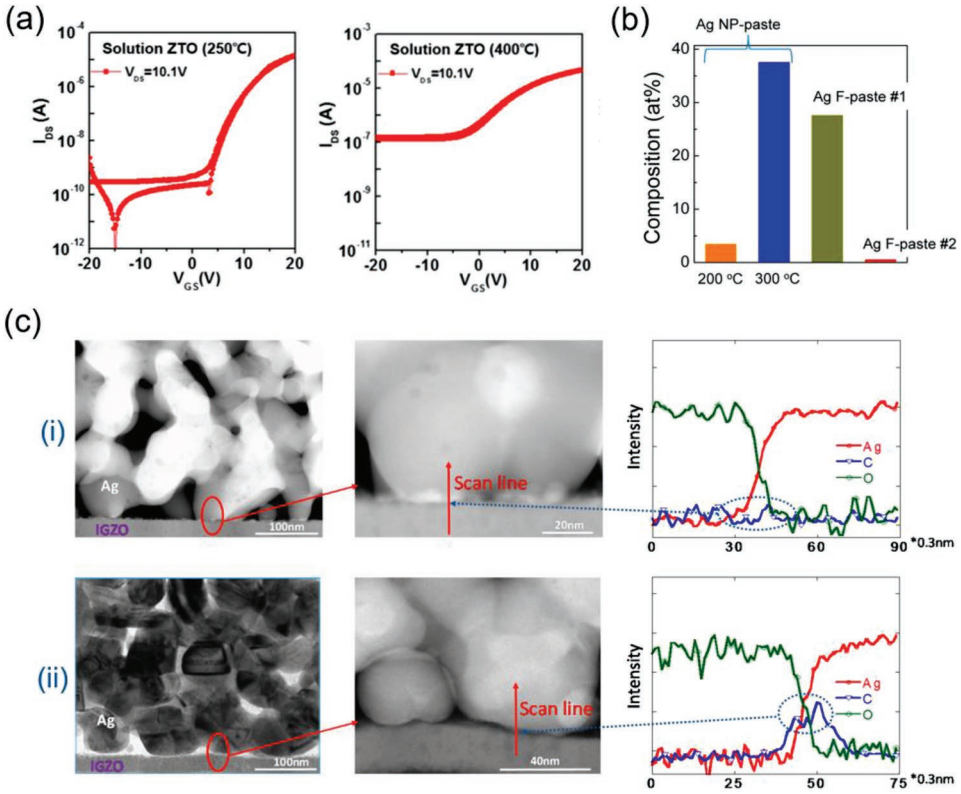

Figure 6. a) Transfer curve characteristics displaying increased drain current when devices are annealed at 400 °C compared to 200 °C, attributed to thermally induced migration of Cu contact material into underlying ZTO semiconductor. Reproduced with permission.[32] Copyright 2016, American Chemical Society. b) XPS results of atomic % Ag in underlying IZO semiconductor, revealing thermally induced Ag migration at 300 °C. Addition of a triblock polymer to a silver paste (Ag F-paste #2) significantly reduces the extent of Ag migration in comparison to a paste without the triblock polymer (Ag F-paste #1). Both pastes were dried at 80 °C. Reproduced with permission.[33] Copyright 2017, American Chemical Society. c) TEM images and EELS measurements showing that an Ag-salt-based ink (i) presents lesser quantities of carbon-based contaminants at the interface with the underlying IGZO than is observed for a nanoparticle-Ag-based ink (ii). Reproduced with permission.[50] Copyright 2017, Multidisciplinary Digital Publishing Institute.

It was found that using large-molecular-weight polyvinylpyrrolidone (PVP) capping molecules enabled modification of Cu NP surface energy by weakening the interfacial dipole at the Cu surface for tailoring of the Cu work function to more closely match that of the solution-processed ZTO semiconductor. This improved charge injection across the contact interface to achieve a low $R_c \times W = 0.092$ MΩ cm. When increasing the annealing temperature from 200 to 400 °C, the authors observed diffusion of Cu into the underlying ZTO, which was detrimental to the TFT performance. The same phenomenon was observed from ROP-patterned Cu ink that was thermally cured under nitrogen across the same temperature range of 200 to 400 °C.[32] In this case, the electrical properties of the printed Cu improved with increasing temperature, reaching $\rho_{S/D} \approx 6.2$ μΩ cm, but the thermally induced Cu migration into the underlying ZTO caused a compromised TFT performance with increased OFF-current as presented in **Figure 6**a. In a different study, diffusion of screen-printed Cu into underlying IGZO caused a high gate leakage current even when cured at a relatively low temperature of 140 °C.[58] This suggests that using a low annealing temperature alone is insufficient for mitigating the migration of printed metal contact material into the underlying semiconductor, and therefore, there is a need for the development of strategies to resolve this issue.

Ag NP and flake-based inks are commercially available for various printing methods, and thus, have been widely investigated in many studies as printed S/D contact material for oxide TFTs. Although Ag is more expensive than Cu, it has the benefit of being more resistant to oxidation, which permits processing in oxygen-containing environments. However, Ag contacts are known to typically suffer from poor charge injection across the interface to oxide semiconductor, resulting from contact resistance caused by a spatial potential barrier, even when the contact material is deposited by electron beam evaporation.[163] This barrier might arise from a work function mismatch between Ag contact and oxide semiconductor.[164] In the case of NP Ag inks, the barrier to charge injection might be worsened by carbonaceous residues from NP capping agents.[49] In 2009, a simple dip-coating lithography process was demonstrated where high-resolution patterning of Ag NP ink was controlled by its interaction with a monolayer of photopatterned octadecyltrichlorosilane to generate a 10 μm TFT channel length.[55] The authors observed a negative shift in V_{on} which they attributed to the migration of Ag into IGZO semiconductors, showing that the problem of metal diffusion into underlying materials is not restricted to Cu-based inks.

Screen-printing of Ag NP ink has been shown to produce TFTs with no observed current crowding, suggesting relatively good contact resistance between Ag contacts and ZTO semiconductors although suffering from mechanical instabilities such as brittleness and poor adhesion.[38] In another study, printed Ag contacts on ZTO were reported to show unstable switching characteristics that were explained by Ag ion migration into the oxide layer.[165] It has also been reported that a relatively good contact into In_2O_3 semiconductor with small hysteresis can be achieved after annealing at much higher temperatures than what is specified for the Ag ink by the material provider.[43] The improved properties were suspected to be due to enhanced field emission caused by Ag-migration spikes in the semiconductor during the annealing step. However, the contacts were not stable over long periods of time of a month or more, again suggesting problems arising from Ag migration.

Direct writing using a dispenser machine has the benefit of low wastage of inks and provides the ability to pattern inks with relatively high viscosities, for instance, those with high loadings of organic polymers, that is not possible with some other non-contact printing methods such as inkjet. The ability to pattern high viscosity inks was exploited in a study where two parallel approaches were pursued in using bulky organic ink additives to suppress the migration of Ag into underlying IZO; i) Ag NPs capped with long chain oleic acid, and ii) a paste formed from Ag flakes (Ag F-paste) containing a thermoplastic triblock copolymer polystyrene-polyisoprene-polystyrene (SIS).[33] The strategy resulted in operational TFTs both when using the Ag F-paste cured at 80 °C, and when the capped, Ag NP material was cured at 200 °C. However, as shown in Figure 6b, X-ray photoelectron spectroscopy (XPS) studies of IZO beneath the printed Ag films revealed that significant Ag diffusion into IZO occurred at an annealing temperature of 300 °C, with thermogravimetric analysis (TGA) of the precursor ink suggesting that the diffusion might be enabled by thermal degradation of the organic capping agent. This study demonstrated how the inclusion of bulky organic species can impede the diffusion of metal contact material into underlying oxide when processing at relatively low temperatures. Organic diffusion-restricting materials decompose at elevated temperatures, and therefore, alternative strategies are required to limit thermally induced migration of metal contact materials into other layers. In addition, contaminants, such as residual carbon from a solvent, might hinder charge injection across the interface between the oxide semiconductor and contact electrodes.[166] When using an alcohol-based solvent system for inkjet printing of NP-based Ag ink, it is possible to reduce the quantity of interfacial carbon impurities by increasing the substrate temperature,[51] however, this also affects the wetting behavior of the ink, which imposes restrictions on print resolution.

One approach for alleviating the use of organic additives is reliance on inks based on silver salts such as silver acetate,[51] silver citrate,[167] or organometallics.[168] When analyzed by electron energy loss spectroscopy (EELS), a silver salt-based ink (TEC-IJ-010, INKTEC, Korea) was employed to fabricate inkjet-printed Ag contacts that presented significantly less accumulation of carbon impurities at the interface of the Ag and IGZO semiconductor than was observed when devices were prepared using an Ag NP based ink (Figure 6c).[50] However, the generated Ag material exhibited a porous structure, which might compromise mechanical durability and lead to a collection of point-like contacts to the semiconductor. In another study investigating the same Ag ink versus sputtered Ag,[12] the bulk of the printed Ag material was also observed by transmission electron microscopy (TEM) to be porous, but there appeared to be an intimate contact for charge injection between IGZO and Ag. In addition, energy-dispersive X-ray spectroscopy (EDS) revealed a clear interface with no evidence for the diffusion of Ag into underlying IGZO or signs of deleterious interfacial chemical interactions. Furthermore, the authors observed that with increasing thickness of IGZO semiconductor, there was a proportional increase in surface roughness and decrease in contact resistance, which might result from better adhesion of printed Ag. However, the printed Ag contacts showed a more pronounced upward-curvature in the low-V_d region of the output characteristics (see Figure 2e) that was suspected to be caused by the higher work-function of the printed Ag (4.87 eV) than that of the sputtered Ag (4.78 eV) as obtained by Kelvin probe measurements.

Improved adhesion between inkjet-printed In_2O_3 and Ag NP contacts was reported by the inclusion of an inkjet-printed polyethyleneimine (PEI)/InO_x composite interfacial film that was observed to reduce the contact resistance by an order of magnitude, acting as an electron transport layer enabling the printed Ag NP film to form an Ohmic contact with underlying In_2O_3 in tandem with improved adhesion.[49] In another example of interfacial engineering, the contact resistance was reduced by two orders of magnitude by adding an interfacial layer of indium tin oxide (ITO) between the ZnO semiconductor and Ag top contacts, with all three layers being patterned by inkjet printing.[97] The authors attribute the improvement to the formation of localized interface states, which act to increase the interfacial charge carrier concentration of the ZnO.[169,170] In another example, interfacial control was demonstrated by the use of Ar plasma treatment to reduce surface trap states such as carboxyl or hydroxyl groups on the IGZO semiconductor surface prior to inkjet patterning of Ag NP contacts.[52]

In addition to Ag NP and Ag salt-based inks, high aspect ratio Ag nanowires (NWs) are another possible approach for generating conductive networks for contact electrodes. Spin-coated Ag NWs have been used in conjunction with inkjet-printed Ag NPs as contact electrodes for an ultrashort vertical channel (around 120 nm) In_2O_3 TFTs, where mechanical durability of the NW network combined with the vertical TFT architecture facilitated much better tolerance to mechanical strain than was observed from a planar device architecture.[53] Ag NWs can also be patterned to act as S/D contacts, as was demonstrated by spray coating through a shadow mask.[54] The authors found that a hot press step (under 3000 psi at 120 °C) reduced the sheet resistance of patterned NWs by 35% and minimized the occurrence of interspaces at the interface between the Ag NWs and underlying IGZO, generating sufficient physical contact for charge injection between the two materials.

A recent study reported screen-printed molybdenum (Mo) NP ink that was cured by intense pulsed light (IPL) irradiation process under ambient conditions. The as-printed Mo ink displayed low electrical conductivity that the authors attributed to an oxide film on the surface of NPs. This was circumvented by

sintering using the IPL irradiation process and enabled high electrical conductivity of 35 μΩ cm. Print-patterned Mo was applied as S/D electrodes for IGZO-based TFTs that displayed mobility of 13.5 cm^2 V s^{-1}.[60]

3.2.2. Printable Conductive Metal-Oxides

An important class of TFT S/D materials is the transparent conductive oxides (TCOs). Such materials may be formed by substitutional doping of an oxide semiconductor with dopant atoms that i) provide excess electrons at the dopant site (n-doping) shifting the Fermi level up within the conduction band to allow electrical conductivity, and ii) increase the apparent band gap through Burstein–Moss shift to enable optical transparency.[53,171] One of the most broadly studied TCOs is ITO (substitutionally Sn-doped indium oxide). TCO-based contacts, such as ITO or H-doped IGZO, are often employed in vacuum-processed IGZO TFTs.[79,102] Despite being less electrically conductive than metals and often requiring a high processing temperature (>300 °C) when deposited from solution, there has been also substantial research into metal oxide-based materials as print-patterned contact electrodes.

ITO can be print patterned to form contact electrodes for oxide TFT devices. In one study, contact resistance observed between inkjet-printed ITO and IGZO was suggested to possibly arise from a difference in the work function of these materials.[39] This problem was tackled by inserting an inkjet-printed interfacial layer of IZO, acting to reduce the contact resistance by providing a material with a higher carrier concentration than that of the IGZO at the interface with the highly conductive ITO.

In the case of precursor-based inks, sufficient densification of oxide and decomposition of residual organic precursors from ITO inks can demand annealing temperatures as high as 500 °C, causing thermally induced material migration, which can lead to increased contact resistance at the semiconductor-contact interface, as reported in ref. [67], due to the migration of inkjet-printed ITO S/D material into the underlying ZTO semiconductor. Furthermore, materials, such as amorphous oxide semiconductors or polymer substrates, do not tolerate such elevated thermal conditions because oxides can crystallize to lose their amorphous phase, and polymer substrates can become deformed or decompose, so the electrical conductivity of oxide S/D material may need to be sacrificed by low-temperature annealing to enable compatibility with such device materials.[40]

One way to reduce the thermal budget required for generating the desired reaction product from the metal oxide precursor route is by solution combustion synthesis (SCS), where an oxidizer, fuel, and a specific temperature are carefully combined as described in a recent review article.[172] The SCS approach was exploited using acetylacetone as the fuel and metal nitrate as the oxidizer to enable the production of ITO contact electrodes at 250 °C for zirconium-indium-zinc-oxide (ZIZO)-based TFTs.[64] Another method for realizing low-temperature fabrication of TCOs is to avoid carbon-based impurities from high boiling point organic solvent systems by use of aqueous-based inks of metal-nitrate precursors, as has been reported for fabrication of inkjet-printed aluminum-doped cadmium oxide (ACO) contact electrodes at 250 °C for InO_x-based TFTs.[71,72] TLM studies of the ACO contacts revealed low contact resistance of around 160 Ω cm, which showed gate voltage dependence, particularly when the semiconductor films were thicker. The authors suggested that the contact resistance was dominated by the bulk resistance of InO_x.

As discussed earlier, the coffee-ring effect[126] can pose challenges for generating uniform material features from liquid-based precursors such as solution or dispersion inks. However, the coffee ring effect can be beneficial when exploited for enabling controlled patterning of subsequently deposited materials. This strategy was employed in the fabrication of InO_x TFTs with channel lengths of only 3.5 μm, by using hydrophobic coffee-ring-type edge features (stripes) of inkjet-printed CYTOP fluoropolymer to define the channel length of subsequently printed ITO S/D contact precursor ink (**Figure 7**a).[68] In a further study by the same group, CYTOP coffee stripes were used for 1) patterning of aluminum oxide-neodymium (AlO_x:Nd) gate electrode by CYTOP acting as a barrier film for selective phosphoric acid etching of outer-lying AlO_x:Nd, and 2) formation of inkjet-printed ITO S/D electrodes self-aligned on either side of the CYTOP due to the hydrophobicity of the fluoropolymer causing dewetting of the ITO ink.[65] In both cases, the CYTOP was subsequently removed by thermal decomposition during the annealing of the ITO layer at 350 °C. Another example where the coffee ring effect was harnessed to assist the fabrication of oxide TFTs reported inkjet-printed ITO, where the center region of the print pattern was thinner (around 10 nm) than the edges (around 15 nm) (Figure 7b).[66] The thinner region of the material displayed semiconductor properties, enabling its use as a channel material for TFTs. The second printing of ITO was then performed over the thicker edges. Upon annealing, the material from the second printing merged with that of the first printing to form electrically conductive S/D contacts.

If the coffee-ring effect is not desired, then it can possibly be circumvented by surface pretreatments, annealing conditions, and using solvent mixtures with different boiling points and viscosities.[173,174] This was demonstrated for the production of fully inkjet-printed transparent oxide TFTs incorporating antimony-doped tin oxide (ATO) gate electrode, ZrO_2 dielectric, SnO_2 semiconductor, and ATO S/D electrodes.[62] Here, the surface of polymethyl methacrylate (PMMA) was treated by UV/ozone to reduce hydrophobicity, and the sample stage was heated for enabling controlled wetting to suppress the extent of the coffee ring effect in ethanol-based oxide precursor inks containing high-viscosity co-solvents. The PMMA material was subsequently removed by thermal decomposition during the annealing of the oxide materials.

In an approach for controlled wetting, selective area deposition was reported by inkjet printing of hydrophobic PMMA polymer patterns onto hydrophilic ZrO_2 surface, providing surface energy contrast for selective area deposition of ATO S/D contact material by spray pyrolysis, with the PMMA material removed by thermal decomposition during annealing of the oxide.[31]

A final selected example of oxide-based S/D electrodes print-patterned by inkjet process includes IZO,[61] where it was found that indium diffused into the underlying ZTO channel during

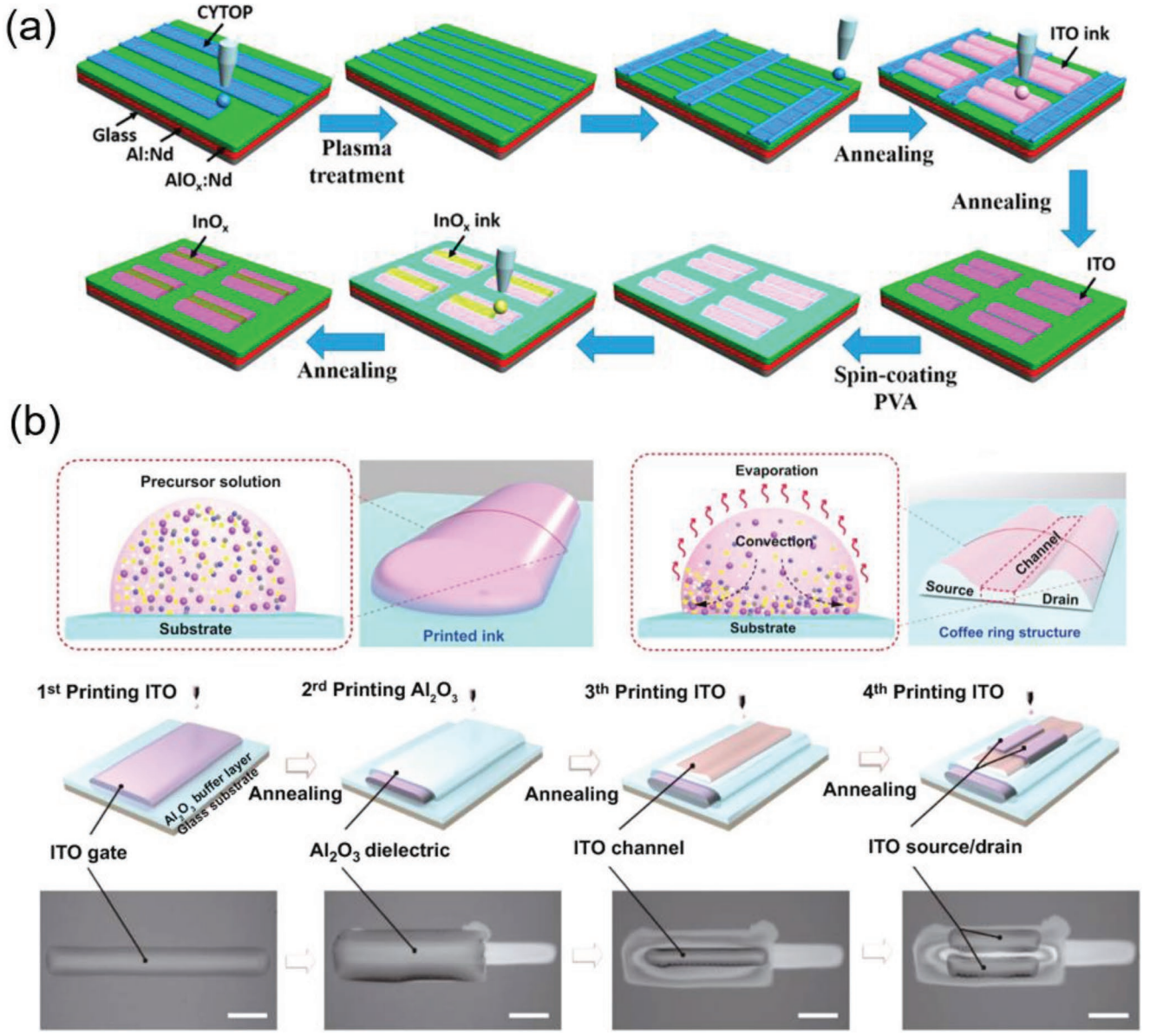

Figure 7. a) Process flow for fabricating an array of InO_x TFTs with inkjet-printed ITO contact electrodes and the channel being defined by coffee-stripe formation at the edges of inkjet-printed CYTOP fluoropolymer. Reproduced with permission.[68] Copyright 2016, American Chemical Society. b) Illustrations depicting the conversion of freshly printed ITO ink into a resulting solid material with a coffee-ring structure, capable of acting as both the semiconductor channel and source/drain electrodes of a fully inkjet-printed TFT device and corresponding optical images shown beneath (scale bars are 200 µm). Reproduced with permission.[66] Copyright 2021, Springer Nature.

annealing of the IZO electrode material. Unlike the problematic diffusion of metallic contact materials described above, this thermally induced migration of indium assisted the formation of a good electrical contact by enhancing the charge carrier concentration, observed as a smaller contact resistance.

Beyond inkjet printing, EHD jet printing of ITO NP ink for S/D electrodes of ZnO TFTs is reported in ref. [175]. With a 500 °C annealing temperature, the authors reported mobility of 0.052 cm^2 V s^{-1} and a good Ohmic contact as observed from output characteristics. Soft lithographic printing (micromolding in capillaries [MIMIC]) of ITO nanoparticle dispersion for S/D electrodes of ZnO transistors is reported in ref. [176]. Here, a PDMS stamp with recessed capillary channels was pressed against the substrate followed by the filling of the capillaries with the ink. High-resolution deposition methods have been used for print-patterning of oxide-based S/D materials for oxide TFTs. For example, rheology printing, in which the pattern is imprinted with a mold at elevated temperature into a uniformly coated material film, can enable well-defined patterning at tens of nanometer resolution,[37] with an alignment accuracy of <5 µm.[63] ROP has also been used to demonstrate sub-micrometer gap (0.2 µm) dimensions for a range of metal

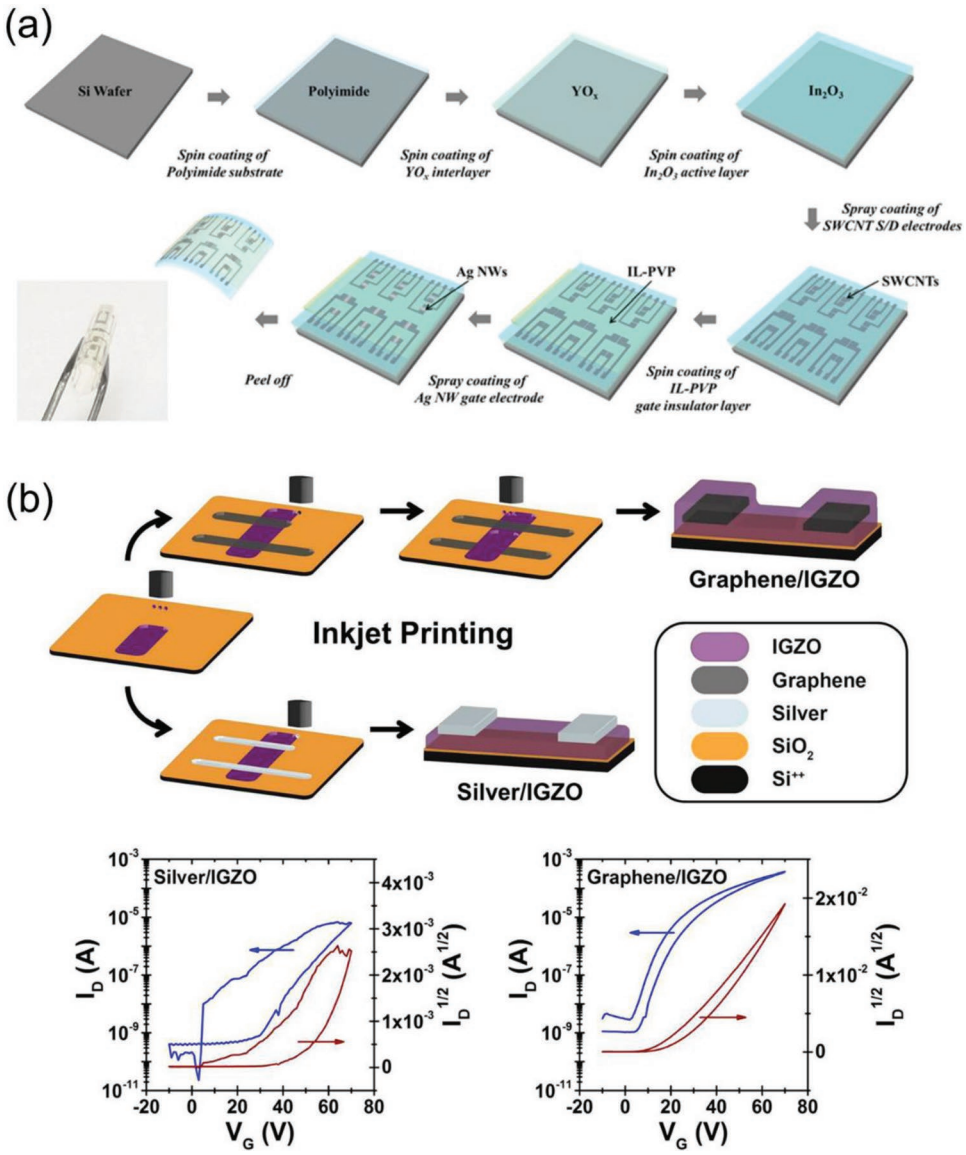

Figure 8. a) Stepwise process flow for production of foldable TFTs incorporating single-walled carbon nanotube contact electrodes patterned by spray coating through a shadow mask. Reproduced with permission.[77] Copyright 2016, American Chemical Society. b) Fabrication process (top) for inkjet-printed graphene or silver contact electrodes with transfer characteristics (bottom) revealing superior electrical performance from the graphene material. Reproduced with permission.[41] Copyright 2016, American Chemical Society.

acetylacetonate inks that could be used for contacts on IGZO TFTs,[13] albeit the TFT devices with hydrogen-doped MoO_x contacts had large feature sizes with $W = 240$ µm and $L = 60$ µm channel dimensions.

3.2.3. Printable Carbon-Based and Other Materials

The electronics sector is amidst a paradigm shift toward the circular economy and resource sustainability. Eco-conscious green values encourage the incorporation of abundant carbon-based materials into TFT devices where possible.[177] This, in addition to low material cost and the possibility for low-temperature solution processing, has motivated the emergence of print-patterned carbon-based S/D materials for oxide TFTs. For instance, patterning of single-walled carbon nanotubes (SWCNTs) was demonstrated by spray coating through a shadow mask onto underlying In_2O_3 semiconductor (**Figure 8**a) resulting in flexible TFT devices which tolerated 1 mm bending radius and folding strain of 26.8% while maintaining the charge carrier mobility at over 79% of its initial value after 5000 cycles of folding in both parallel and perpendicular directions.[77] Another report[41] studied inkjet-printed graphene S/D contacts with inkjet-printed IGZO, where TFT transfer characteristics suggested that a more chemically stable electrode/semiconductor interface was formed using graphene than when using an Ag NP-based ink (Figure 8b). This is supported by an earlier study

where graphene was shown to perform well as a stable interfacial barrier material for retarding the oxidation of Al contacts caused by the diffusion of oxygen from underlying IGZO.[178] Recently, carbon ink was screen-printed as contacts for electrolyte-gated ZnO TFTs,[179] where an in-plane device architecture enabled the fabrication of both S/D and gate electrodes in a single printing step, with the processing of all device components being performed in air with a low thermal budget of 150 °C.

When used as S/D electrode materials for TFTs, carbon-based materials can suffer from contact problems at the interface with oxide semiconductors, which has been explained by the high work function of carbon materials.[180–182] Carbon materials may be combined with other materials to modulate their work function/Schottky barrier for applicability in oxide TFTs. This approach was employed by spray coating SWCNTs through a shadow mask onto a film of AZO NPs used as S/D contacts with In_2O_3 semiconductors in flexible TFTs.[78] This study exploited the low work function of the AZO component for tuning the work function of the SWCNT-AZO hybrid to 4.6 eV, which enabled Ohmic contact between the semiconductor and S/D contact material. Another method for adjusting the work function of carbon contact material was employed by combining graphene with gold for wet-transfer printing of S/D electrodes for IGZO TFTs.[73] The PDMS stamp transfer printing process enabled a linewidth resolution of 5 µm for the contact material. In a different study, a hybrid material of multiwalled carbon nanotubes (MWCNTs) and PSS directly drawn by the EHD jet printing method was used to form S/D contacts on ZnO semiconductor for fabrication of TFTs with negligible hysteresis.[75]

In addition to the above-described examples of metal, metal-oxide, and carbon-based materials, alternative materials are being explored for their application as S/D contacts for oxide TFTs. Titanium carbide (MXene) possesses metal-like electrical conductivity, with a work function of 4.6 eV providing negligible band offsets from that of ZnO semiconductor to enable Ohmic contact formation when patterned onto underlying ZnO by spray coating and lift-off process.[34] In another demonstration of ZnO semiconductor, Ag NWs together with PEDOT:PSS was patterned by spray-coating through a shadow mask to produce material for S/D electrodes on hysteresis-free TFT devices with a low operating voltage of <3 V and visible optical transparency of around 80%.[76]

3.2.4. Vacuum-Deposited Print-Patterned Metals

To leverage the benefits of vacuum-deposited metals, such as increased conductivity, uniform contact area, and reduced migration, by alleviating the need for a high-temperature annealing step when compared to contacts based on directly printed NPs or metal oxide precursors (Sections 3.2.1. and 3.2.2. above), print patterning can also be achieved by printing a patterned lift-off[43,80] or etching resist[83] before or after uniform deposition of a metal layer, for example, by vacuum evaporation, correspondingly. Alternatively, directly printing an etching ink could be explored for similar advantages.[183] This way, a wider selection of high-quality, bulk-like, and also low-work-function metals, such as Al and Ti, can be fabricated than is possible by using metal inks. In addition, such methods could allow the use of bilayer S/D-contacts where a protective layer of an inert metal (e.g., Au) is deposited on top of a reactive metal providing optimal contact (e.g., Ti) to the oxide semiconductor.[102] For example, evaporated print-patterned aluminum can be used to obtain a stable Ohmic contact with a metal-oxide-semiconductor as reported based on high-resolution ROP of a sacrificial polymer resist for the lift-off process in refs. [80,81] (**Figure 9**). Here, the patterned features of uniform thickness displayed sharp sidewalls with low line edge roughness and linewidths as low as ≈1 µm.

Another similar process known as chemical lift-off lithography (CLL) was demonstrated for the patterning of Au S/D electrodes.[82] In CLL, a self-assembled monolayer (SAM) of hydroxyl-terminated alkanethiols is deposited on top of a uniform Ti/Au layer and patterned by selectively removing a portion of the SAM using micro-contact printing with a plasma-treated, relief-patterned PDMS stamp. The remaining SAM layer is then used as an etch mask for patterning the Ti/Au electrode through wet etching followed by the removal of the SAM layer. The authors report that in contrast to conventional microcontact printing, CLL avoids both lateral diffusion and gas-phase deposition of ink molecules, enabling high fidelity and precision patterning of sub-micrometer scale feature sizes over large areas.

An approach for controlled wetting of S/D material reported the patterning of aluminum zinc oxide AZO contacts by selective area ALD deposition.[70] Here, an inkjet-printed PVP inhibition layer was exploited for patterning of AZO contact material produced by area-selective ALD only in the regions devoid of PVP, resulting in patterned AZO S/D contacts on underlying ZnO semiconductor. The PVP layer was then removed by plasma treatment.

In a process for sputtered a-IGZO TFTs utilizing substrate conformal imprint lithography (SCIL) of top gate electrode resist and wet etching, self-aligned S/D electrodes can be achieved to allow close-to-zero gate and S/D overlaps.[79] A three-layer stamp consisting of PDMS layers with varied Young's moduli was used to ensure conformal contact of the stamping tool and used to pattern a UV-curable imprinting resist on top of the blanket-deposited Mo gate layer. The gate and the underlying gate dielectric (SiO_2) were then patterned through the imprinted resist mask via wet and dry etching, respectively. The patterned top gate/gate dielectric-stack was used as a mask for H-doping of the IGZO semiconductor up to ≈4×10^{19} cm^{-3} charge carrier concentration in the area exposed to NH_3 plasma. IGZO TFTs with channel lengths as short as 450 nm were successfully fabricated with electrical performance on-par with self-aligned devices patterned using conventional photolithography. Through gated-TLM measurements (see Figure 3e), ΔL ≈140 nm was obtained, which indicated that the electrical channel length is shorter than the geometrical gate length, possibly due to lateral diffusion of the H-dopant underneath the gate electrode. Although the process has been used for vacuum-deposited oxide TFTs, the work demonstrates the powerful combination of print-patterning and vacuum-deposition in the fabrication of S/D electrodes to metal oxide TFTs.

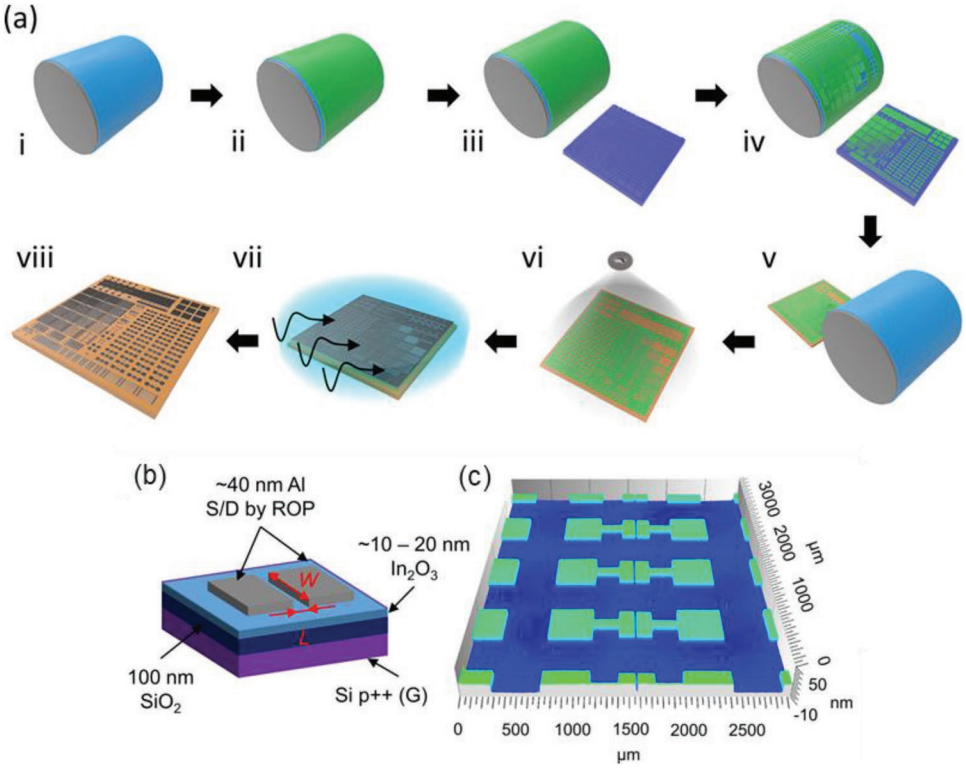

Figure 9. a) Schematic image of the process for metal electrodes patterned using ROP of sacrificial polymer resist, vacuum-deposition (evaporation or sputtering), and lift-off: i) PDMS blanket, ii) polymer resist coating, iii) high-resolution printing plate (cliché), iv) patterning of semi-dry polymer resist, v) transferring of patterned polymer resist to the substrate, vi) vacuum deposition of metal contact, vii) lift-off in an ultrasonic bath in an organic solvent, and viii) final pattered metal structure. b) Schematic image and c) optical profiler map of TFTs with Al contacts patterned using ROP-based lift-off process. Reproduced with permission.[80] Copyright 2021, American Chemical Society.

4. Outlook and Future Perspectives

The materials and processes of printed electronics are evolving to offer an alternative to conventional electronics manufacturing steps that can help to enhance the product form factor (flexibility, stretchability, areal coverage), enable new more sustainable materials to be used, lower the energy and materials consumption of processing, and thereby its environmental footprint.[184–189] Printed TFT applications that depend on this development include active-matrix backplanes of displays and sensor arrays, biosensors, and integrated circuits for sensor data readout and wireless communication. For these applications, print-patterned oxide materials are a promising choice due to their potentially high electrical performance and environmental stability. Toward this end, the electrical performance, stability, and low-temperature processability of printable and print-patternable materials, matching of the materials interfaces, and enhancing the accuracy of the processing to micrometer level and beyond are taking place. High-resolution printing techniques with high alignment accuracy are especially critical for the TFT operation of printed circuits at MHz frequencies. The mobility of the charge carriers in the semiconducting channel (μ), the channel length (L), and the overlap of the gate and S/D electrodes (L_{OL}), together with the operation voltage (V_{GS}) and threshold voltage (V_t), determine the theoretical cut-off frequency (or unity-current-gain frequency, f_T) of a TFT circuit.[190,191] For example, assuming $\mu = 5$ cm^2 V s^{-1}, $V_{GS} = 5$ V, and $V_t = 0$ V, we find that for the TFT circuits to operate at frequencies of $f_T \gg 10$ MHz, both the resolution (that defines L) and the alignment accuracy (that defines L_{OL}) need to be $L, L_{OL} \ll 10$ µm and preferably ≈1 µm. As compared to vacuum deposition, solution processing also has some unique characteristics that in some cases present a problem but sometimes can be used to advantage, like the coffee-ring effect that is discussed in the text. In this review, we focus on the source/drain contacts of oxide TFTs reviewing the approaches, achievements, and challenges in the different materials and processing routes and paying special attention to the characterization methods of the contacts. The material and processing approaches are tabulated in detail in Table 1 and summarized in Tables 2 and 4.

Printed S/D contact electrodes for oxide TFTs typically suffer from problems that are detrimental to device performance such as the modest resolution of printing processes, Schottky contact, large contact resistance, migration of contact material into semiconductor, poor adhesion to semiconductor, long transfer length, and hysteretic behavior under voltage cycling. Various strategies have evolved to combat these challenges, although there does not appear to be a general all-purpose approach. Table 3 summarizes the effects and their possible counter measures. Many of the reports involving printed S/D contact materials based on metal NPs or metal oxides experience challenges with the contact material migrating to the oxide

semiconductor during the high-temperature annealing step that is necessary to convert the printed material into a solid thin film of the right composition and electrical characteristics. One approach is to use organic layers to limit the migration or alleviate the need for annealing by using print-patterned vacuum-deposited layers (evaporated, sputtered, or ALD-grown), that is, thin-films that are patterned using printed lift-off resist, etching masks, etching ink or growth-inhibitor layers, or alternatively, exploring area-selective doping through print-patterned layers. Furthermore, as can be observed from the collection of published reports in Table 1, there is variation in the methods used to assess the performance of printed contacts, hindering the ability for cross-comparison of different achievements.

It can be concluded from this review that the implementation of standardized definitions and procedures could be harnessed to assist in the characterization of printed contacts.[84] This would be particularly important for process control when evaluating upscaled and large-volume production with yield targets. Some proposed examples of standard procedures that could be applicable for evaluating printed S/D contacts for oxide TFTs include i) measurement of I/V transfer and output curves in both directions to indicate the extent of hysteresis loops, ii) use of TLM and gated TLM to investigate contact resistance, semiconductor sheet resistance and transfer length, and iii) examine output curves for nonlinearity at low I_d caused by a Schottky barrier or space-charge-limited current (current-crowding). Adoption of systematic and standardized characterization methods such as these would assist the comparison of different device fabrication approaches, to help identify benefits or pitfalls in methods, and ultimately accelerate the progress of printed S/D contacts for oxide TFTs.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

metal-oxide semiconductors, printed electronics, printed transistors, source/drain contacts, thin-film transistors

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